HT32F57331/HT32F57341
HT32F57342/HT32F57352
Datasheet

32-Bit Arm® Cortex®-M0+ USB LCD Microcontroller, up to 128 KB Flash and 16 KB SRAM with 1 Msps ADC, DAC, CMP, DIV, USART, UART, SPI, I²S, I²C, GPTM, PWM, SCTM, BFTM, SCI, CRC, RTC, WDT, LCD, PDMA, AES-128 and USB2.0 FS

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1 General Description

The Holtek HT32F57331/57341/57342/57352 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The devices operate at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and up to 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as USB2.0 FS, PDMA, AES-128, Hardware Divider DIV, SPI, I^2S, USART, UART, SCI, I^2C, GPTM, PWM, SCTM, BFTM, CRC-16/32, RTC, WDT, ADC, CMP, DAC, LCD and SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application controllers, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor controllers and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option storage
- Up to 16 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F57331/41/42/52 series devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator to obtain maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±1 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated clock PLL and USB PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{DD} and V_{CORE} power domains
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 10 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in these devices. There are multiplexed channels, which include up to 10 external analog signal channels and 4 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D Conversion can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (V_{REF}) which can provide a stable reference voltage for the A/D Converter and Comparators is internally connected to the ADC input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

Comparator – CMP

- Rail-to-rail comparators
- Configurable negative inputs used for flexible voltage selection
  - External CN pin
  - Internal 8-bit CVR output
- Programmable hysteresis
- Programming respond speed and consumption
- Comparator output can be routed to I/O pin, to multiple timers or ADC trigger inputs
- 8-bit CVR can be configurable to dedicated I/O for voltage reference
- Comparator has interrupt generation capability with wakeup from Sleep, Deep-Sleep1 or Deep-Sleep2 mode through the EXTI controller

The two general purpose comparators, CMP, are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the CPU from the Sleep, Deep-Sleep1 or Deep-Sleep2 mode through the EXTI wakeup event management unit.

Digital to Analog Converter – DAC

- Two DAC converters with each having one output channel
- 12-bit or 8-bit resolution
- Maximum 500 ksps conversion updating rate
- Dual DAC channels for implementing simultaneous conversion
- Supports voltage output buffer mode and bypass voltage output buffer mode
- Reference voltage from internal reference voltage V_{REF} or V_{DDA}

The DAC Module has two Digital to Analog Converters. Each is a 12-bit, voltage output digital to analog converter and has one output channel. The DAC can be configured in 8-bit or 12-bit mode. The DAC conversion could be implemented independently or simultaneously when both channels are grouped together for synchronous update operation.

I/O Ports – GPIO

- Up to 67 GPIOs
- Port A, B, C, D, E are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 67 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a quadrature decoder with two inputs.

Pulse-Width-Modulation Timer – PWM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse-Width-Modulation Timer, PWM, consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, i.e., when the device enters the power-saving mode, the RTC counter is used as a wakeup timer to let the system resume from the power saving mode.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detection and clock synchronization function to prevent the situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programming baud rate clock frequency up to (f_{PCLK}/16) MHz for Asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS

- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character Transfer mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (Elementary Time Unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and check functions
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface, SCI, is compatible with the ISO 7816-3 standard. This interface includes functions for Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Inter-IC Sound – I²S

- Master or Slave mode
- Mono and Stereo
- I²S-justified, Left-justified and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 × 32-bit TX & RX FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I²S supports a variety of data formats. In addition to the stereo I²S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I²S operates in the master mode, using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:
  ADC, SPI, USART, UART, SCI, I²C, I²S, GPTM, PWM, AES-128 and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by controlling the “START” bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Liquid Crystal Display Controller – LCD

- LCD Driver function with Static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty
- LCD Driver function with Static, 1/2, 1/3 or 1/4 bias
- Supports R type bias type
- Clock source can be selected from the LSI (32 kHz), LSE (32.768 kHz) or a clock ratio of either the HSI or HSE
- Contains three embedded LCD bias reference resistor ladders
- Double buffered memory
- Software selectable charge pump voltage
- Programmable dead time between frames – up to 7/2 phase periods for type A waveforms and 7 phase periods for type B waveforms
- Software selectable waveform type: type A or type B waveform
- LCD frame interrupt
- Blink capability: Up to 1, 2, 3, 4, 8 or all pixels which can be programmed to blink

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays. It includes up to 8 common terminals and 37 segment terminals to drive 148 (4 commons × 37 segments) or 264 (8 commons × 33 segments) LCD picture elements (pixels). The exact number of terminals depends on the device package pin out. An integrated charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 Full-Speed (12 Mbps) specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffers. Each endpoint buffer size is programmable using corresponding registers, thus providing maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Advanced Encryption Standard – AES-128

- Supports AES Encrypt / Decrypt functions
- Supports AES ECB/CBC/CTR modes
- Supports Key Size of 128 bits
- Supports 4 words Initial Vector for CBC and CTR modes
- 4 × 32 bits AES data buffer
- Supports PDMA interface
- Supports Word Data Swap function

The AES core supports both encryption and decryption functions and supports 128-bit input data. It should be noted that hardware does not pad out any input data bits, therefore users need to do pad action by software at first.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 48/64-pin LQFP packages for HT32F57331/HT32F57341
- 48/64/80-pin LQFP packages for HT32F57342/HT32F57352
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F57331	HT32F57341	HT32F57342	HT32F57352
Main Flash (KB)		32	63	64	127
Option Bytes Flash (KB)		1	1	1	1
SRAM (KB)		4	8	8	16
Timers	GPTM	1		1	
	PWM	2		2	
	SCTM	—		2	
	BFTM	2		2	
	WDT	1		1	
	RTC	1		1	
Communication	USB	1		1	
	SPI	2		2	
	USART	1		1	
	UART	2		2	
	I^2C	2		2	
	I^2S	—		1	
	SCI (ISO7816-3)	1		2	
PDMA		—		6 channels	
AES-128		—		1	
Hardware Divider		1		1	
LCD (COM × SEG)		Up to 8 × 25, 6 × 27, 4 × 29		Up to 8 × 33, 6 × 35, 4 × 37	
CRC-16/32		1		1	
EXTI		16		16	
12-bit ADC Number of channels		1		1	
		Max. 10 Channels		Max. 10 Channels	
Comparator		—		2	
DAC		—		2	
GPIO		Up to 53		Up to 67	
CPU frequency		Up to 60 MHz		Up to 60 MHz	
Operating voltage		1.65 V ~ 3.6 V		1.65 V ~ 3.6 V	
Operating temperature		-40 °C ~ 85 °C		-40 °C ~ 85 °C	
Package		48/64-pin LQFP		48/64/80-pin LQFP	

Block Diagram

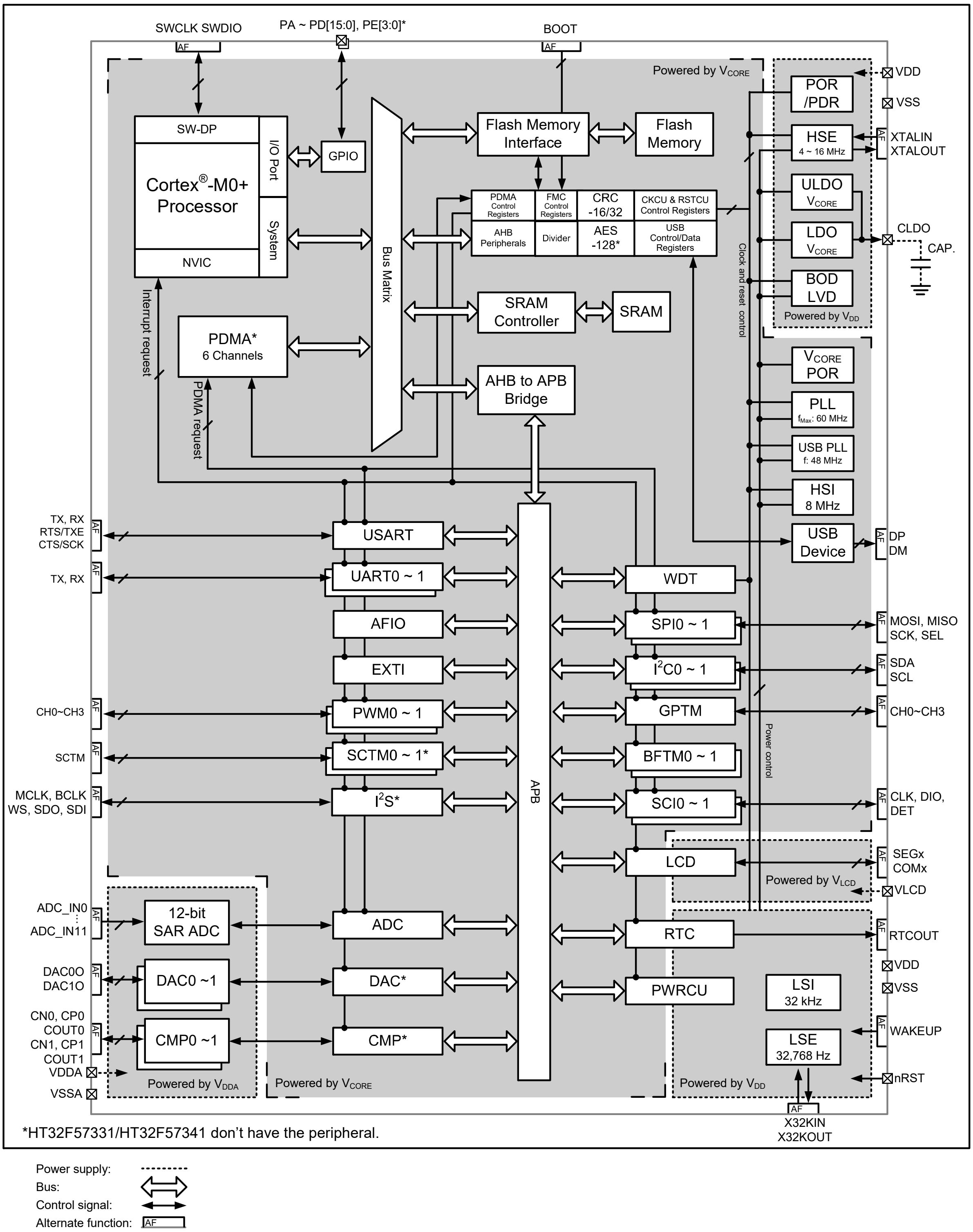


Figure 1. Block Diagram

Memory Map

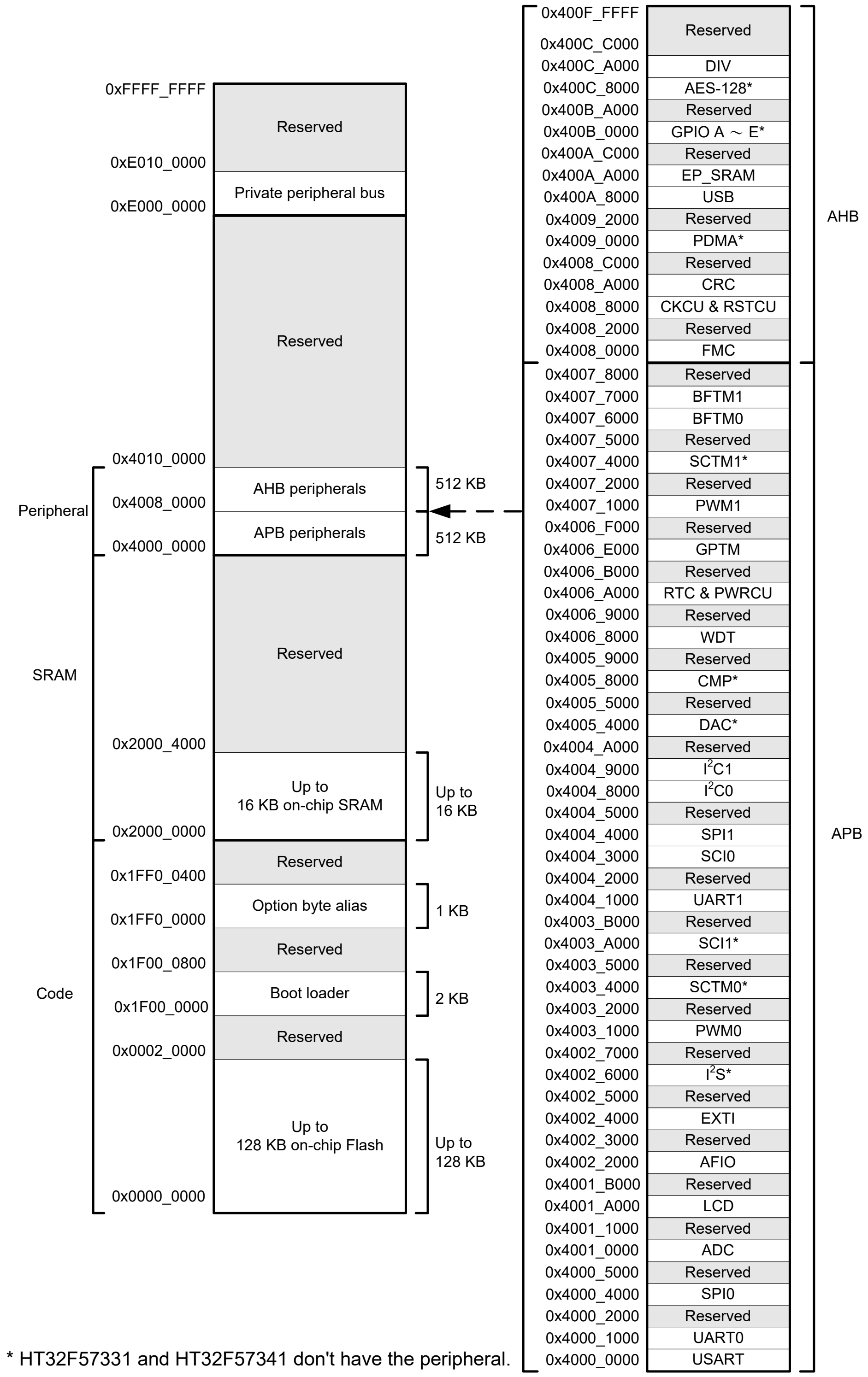


Figure 2. Memory Map

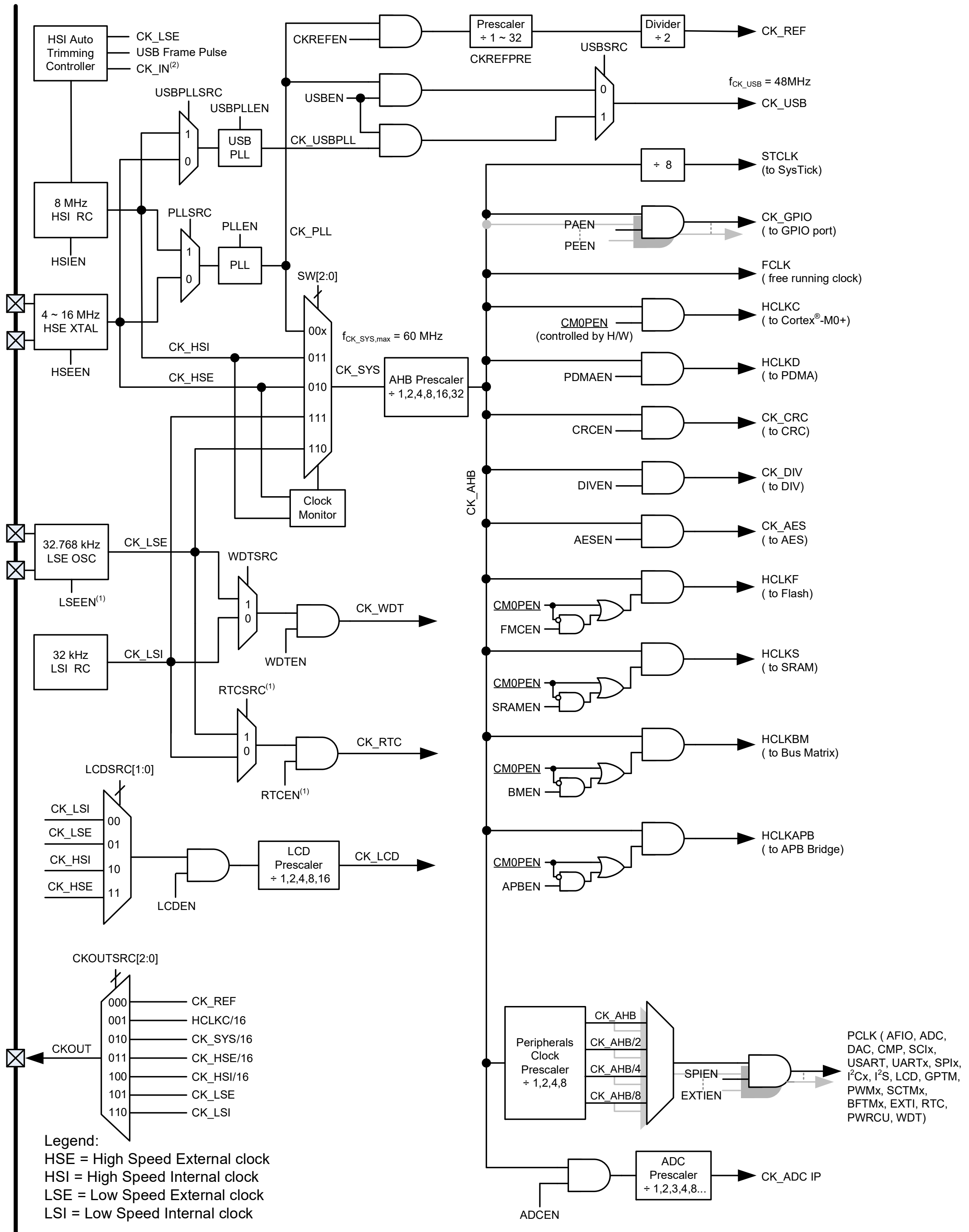
Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_9FFF	Reserved	
0x4001_A000	0x4001_AFFF	LCD	
0x4001_B000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_5FFF	Reserved	
0x4002_6000	0x4002_6FFF	I^2S*	
0x4002_7000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0*	
0x4003_5000	0x4003_9FFF	Reserved	
0x4003_A000	0x4003_AFFF	SCI1*	
0x4003_B000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI0	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4005_3FFF	Reserved	
0x4005_4000	0x4005_4FFF	DAC*	
0x4005_5000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP*	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	

Start Address	End Address	Peripheral	Bus
0x4007_2000	0x4007_3FFF	Reserved	APB
0x4007_4000	0x4007_4FFF	SCTM1*	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA*	
0x4009_2000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB	
0x400A_A000	0x400A_BFFF	EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	GPIO D	
0x400B_8000	0x400B_9FFF	GPIO E*	
0x400B_A000	0x400C_7FFF	Reserved	
0x400C_8000	0x400C_9FFF	AES-128*	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

*: HT32F57331 and HT32F57341 don't have the peripheral.

Clock Structure



Note: 1. Those control bits are located in the RTC Control Register (RTCCR).
2. The CK_IN signal is sourced from the external CKIN pin.

Figure 3. Clock Structure

4 Pin Assignment

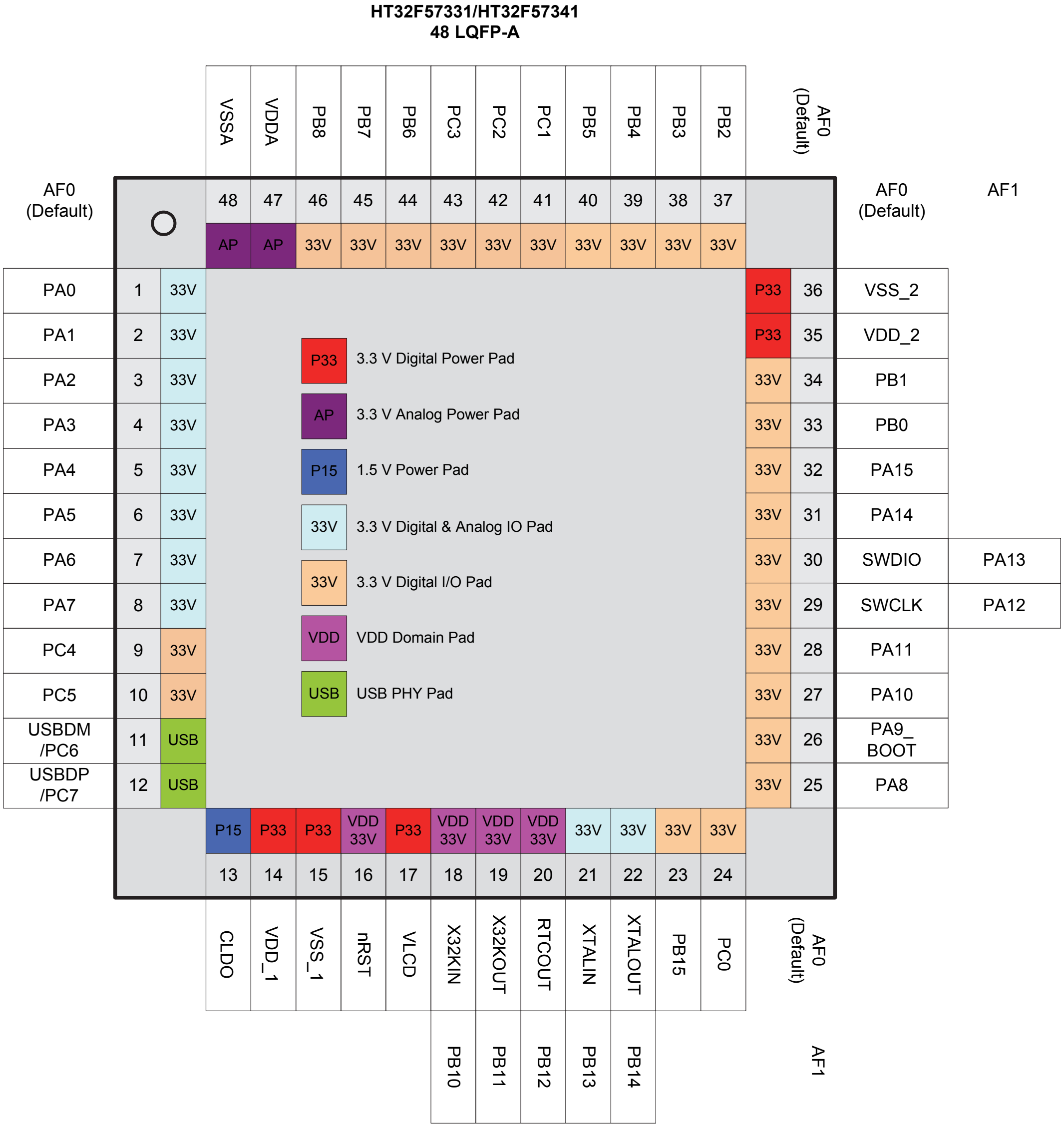


Figure 4. HT32F57331/HT32F57341 48-pin LQFP Pin Assignment

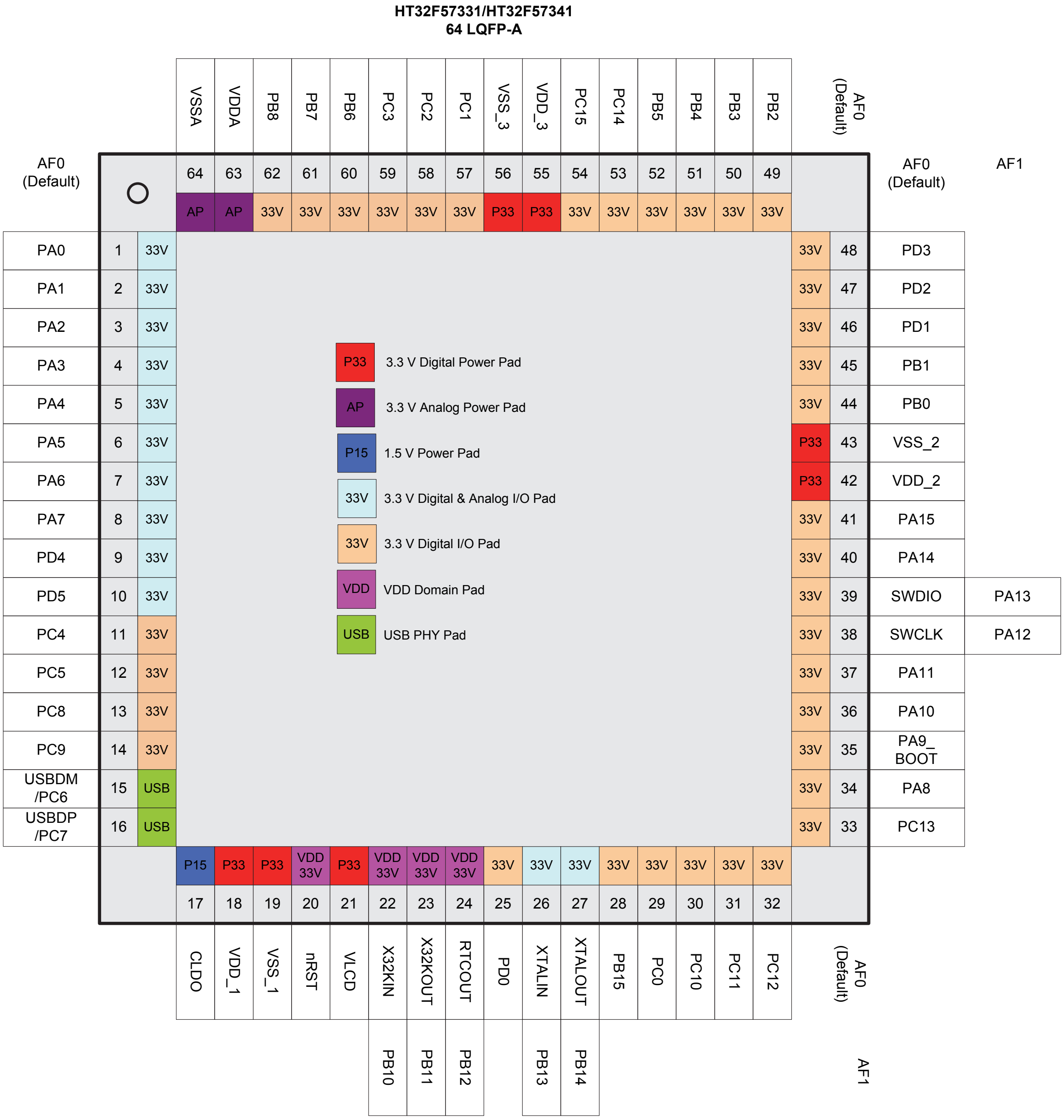


Figure 5. HT32F57331/HT32F57341 64-pin LQFP Pin Assignment

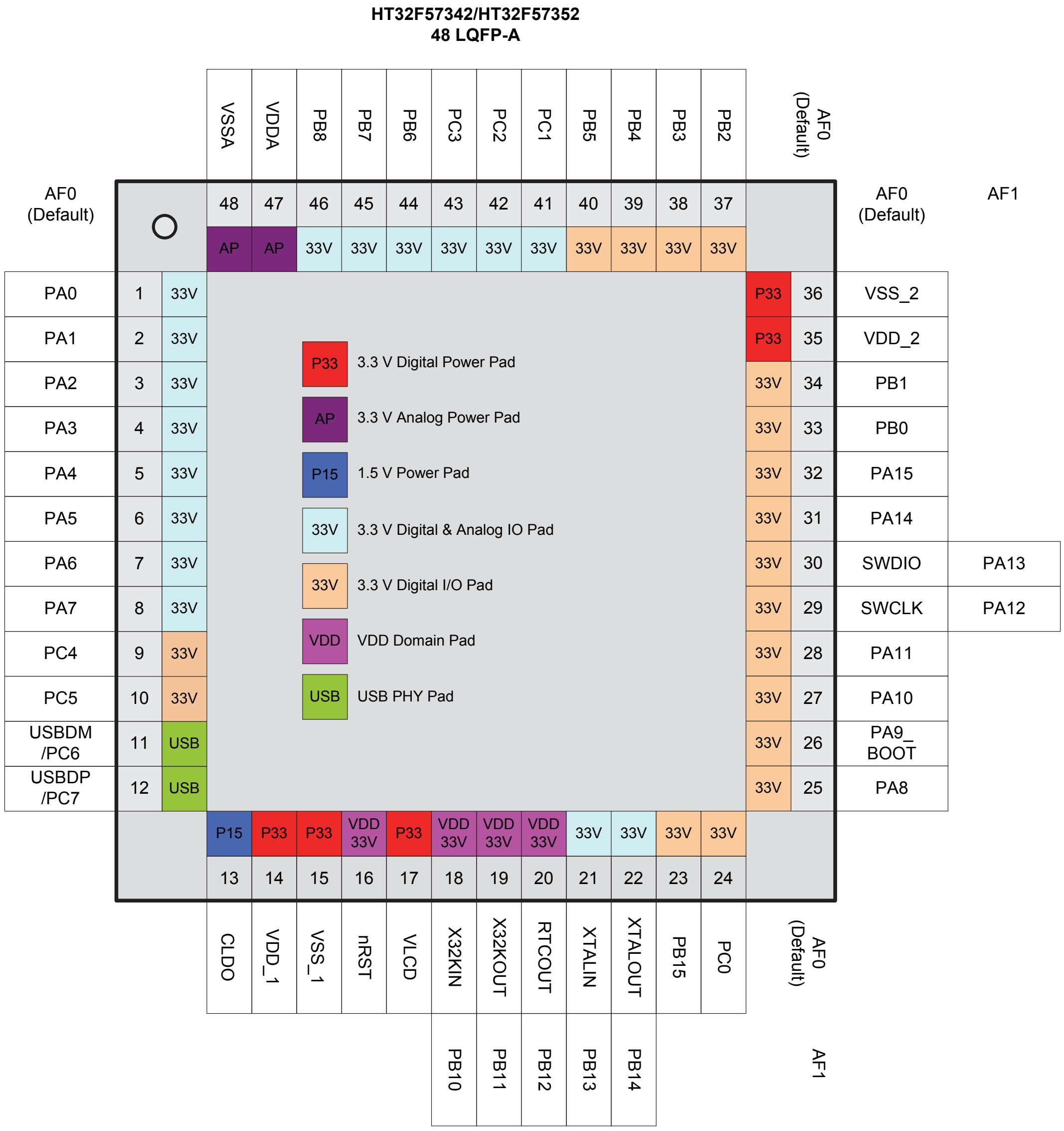


Figure 6. HT32F57342/HT32F57352 48-pin LQFP Pin Assignment

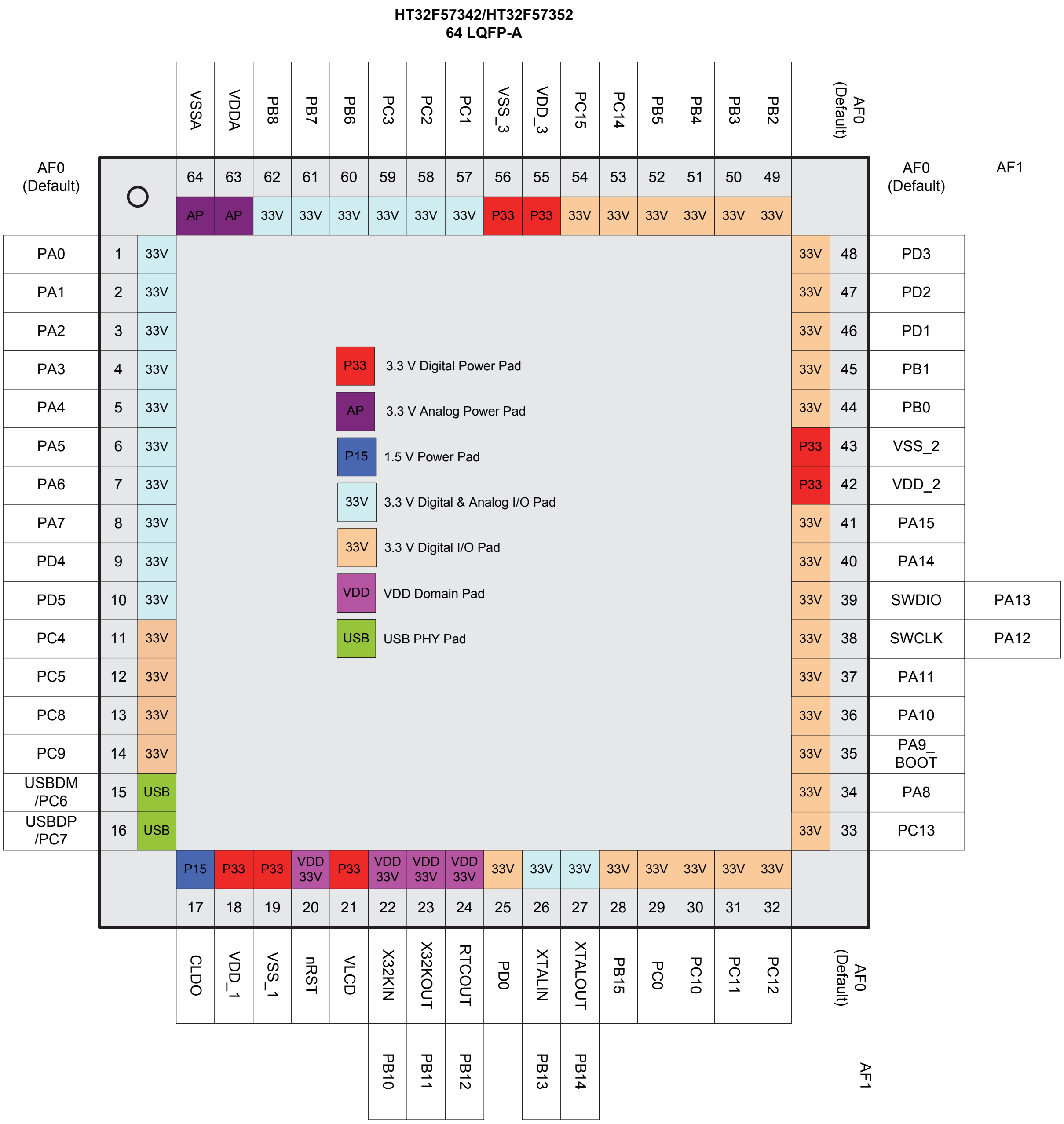


Figure 7. HT32F57342/HT32F57352 64-pin LQFP Pin Assignment

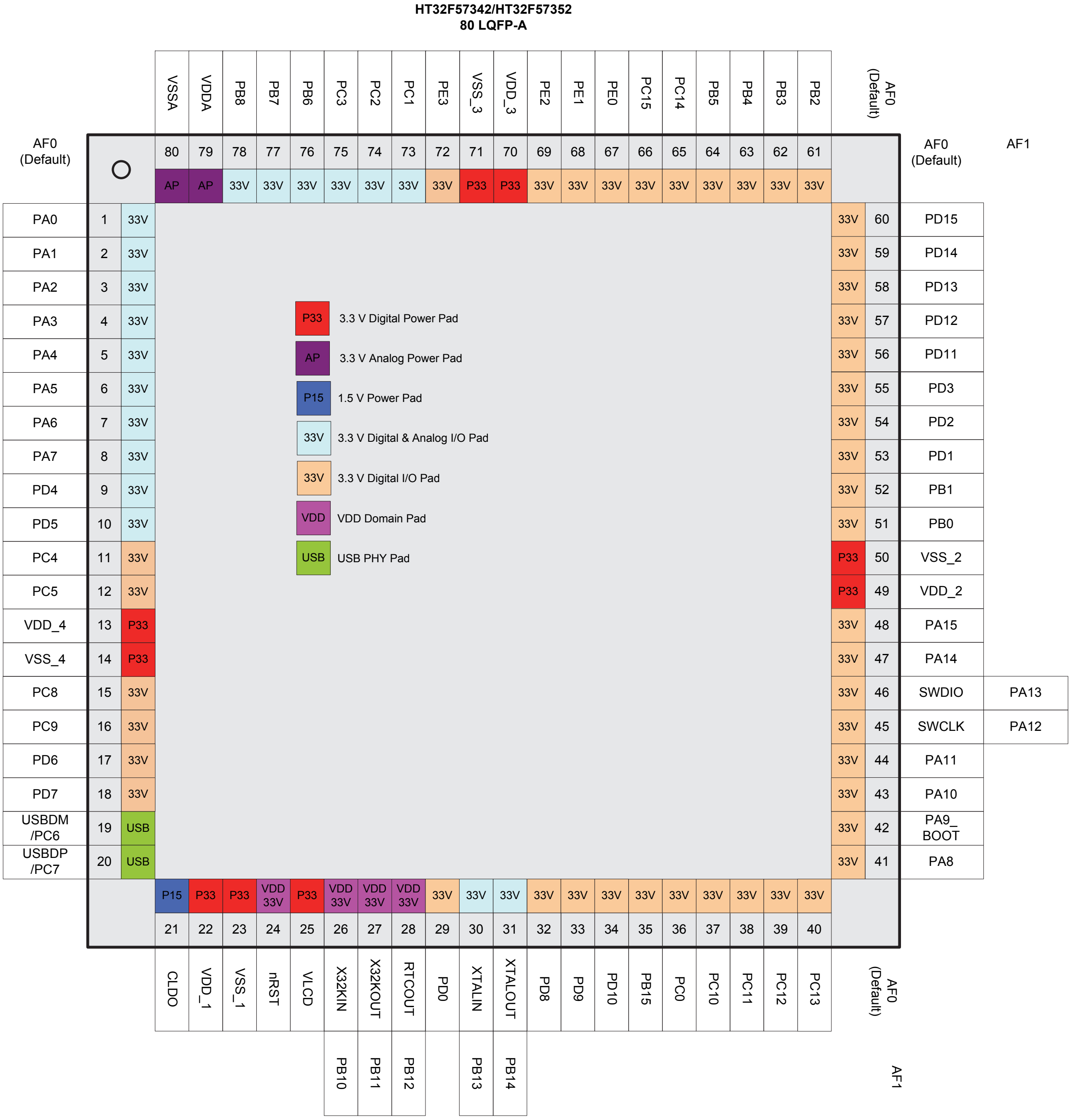


Figure 8. HT32F57342/HT32F57352 80-pin LQFP Pin Assignment

Table 3. HT32F57331/HT32F57341 Pin Assignment

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	SCI	N/A	N/A	N/A	N/A	PWM	LCD	System Other
1	1	PA0		ADC_IN0		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL	SCI_CLK							VREF
2	2	PA1		ADC_IN1		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA	SCI_DIO							
3	3	PA2		ADC_IN2		GT_CH2	SPI1_MISO	USR_TX									
4	4	PA3		ADC_IN3		GT_CH3	SPI1_SEL	USR_RX									
5	5	PA4		ADC_IN4		GT_CH0	SPI0_SCK	USR_TX	I2C0_SCL	SCI_CLK							
6	6	PA5		ADC_IN5		GT_CH1	SPI0_MOSI	USR_RX	I2C0_SDA	SCI_DIO							
7	7	PA6		ADC_IN6		GT_CH2	SPI0_MISO	USR_RTS		SCI_DET							
8	8	PA7		ADC_IN7		GT_CH3	SPI0_SEL	USR_CTS									
9		PD4		ADC_IN8				UR1_TX							PWM1_CH0		
10		PD5		ADC_IN9				UR1_RX							PWM1_CH1		
11	9	PC4				GT_CH0	SPI1_SEL	USR_TX	I2C1_SCL							SEG11	
12	10	PC5				GT_CH1	SPI1_SCK	USR_RX	I2C1_SDA							SEG12	
13		PC8				GT_CH2	SPI1_MOSI	UR1_TX								SEG13	
14		PC9				GT_CH3	SPI1_MISO	UR1_RX								SEG14	
15	11	PC6						UR0_TX	I2C0_SCL								
15	11	USBDM															
16	12	USBDP															
16	12	PC7						UR0_RX	I2C0_SDA								
17	13	CLDO															
18	14	VDD_1															
19	15	VSS_1															
20	16	nRST															
21	17	VLCD															
22	18	X32KIN	PB10					USR_TX									
23	19	X32KOUT	PB11					USR_RX									
24	20	RTCOUT	PB12														WAKEUP
25		PD0							I2C0_SDA							SEG15	
26	21	XTALIN	PB13														
27	22	XTALOUT	PB14														
28	23	PB15					SPI0_SEL	USR_TX	I2C1_SCL						PWM0_CH2	COM0	
29	24	PC0					SPI0_SCK	USR_RX	I2C1_SDA						PWM0_CH3	COM1	
30		PC10				GT_CH0	SPI1_SEL									SEG25/COM4	
31		PC11				GT_CH1	SPI1_SCK									SEG26/COM5	

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I^2C	SCI	N/A	N/A	N/A	N/A	PWM	LCD	System Other
32		PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL							SEG27/COM6	
33		PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C0_SDA							SEG28/COM7	
34	25	PA8						USR_TX							PWM1_CH3	COM2	
35	26	PA9_BOOT					SPI0_MOSI								PWM1_CH2		CKOUT
36	27	PA10						USR_RX		SCI_DET					PWM0_CH1	COM3	
37	28	PA11					SPI0_MISO									SEG0	
38	29	SWCLK	PA12														
39	30	SWDIO	PA13														
40	31	PA14					SPI1_SEL	USR_RTS	I2C1_SCL	SCI_CLK					PWM0_CH0	SEG1	
41	32	PA15					SPI1_SCK	USR_CTS	I2C1_SDA	SCI_DIO						SEG2	
42	35	VDD_2															
43	36	VSS_2															
44	33	PB0					SPI1_MOSI	USR_TX	I2C0_SCL						PWM0_CH1	SEG3	
45	34	PB1					SPI1_MISO	USR_RX	I2C0_SDA						PWM1_CH1	SEG4	
46		PD1						USR_RTS		SCI_CLK						SEG16	
47		PD2						USR_CTS		SCI_DIO						SEG17	
48		PD3								SCI_DET						SEG18	
49	37	PB2					SPI0_SEL	UR0_TX							PWM0_CH2	SEG5	CKIN
50	38	PB3					SPI0_SCK	UR0_RX								SEG6	
51	39	PB4					SPI0_MOSI	UR1_TX								SEG7	
52	40	PB5					SPI0_MISO	UR1_RX								SEG8	
53		PC14							I2C0_SCL							SEG9	
54		PC15							I2C0_SDA							SEG10	
55		VDD_3															
56		VSS_3															
57	41	PC1					SPI1_SEL	UR1_TX							PWM0_CH0	SEG19	
58	42	PC2					SPI1_SCK								PWM1_CH0	SEG20	
59	43	PC3					SPI1_MOSI	UR1_RX							PWM1_CH2	SEG21	
60	44	PB6					SPI1_MISO	UR0_TX		SCI_CLK						SEG22	
61	45	PB7							I2C1_SCL	SCI_DET					PWM0_CH3	SEG23	
62	46	PB8						UR0_RX	I2C1_SDA	SCI_DIO					PWM1_CH3	SEG24	
63	47	VDDA															
64	48	VSSA															

Table 4. HT32F57342/HT32F57352 Pin Assignment

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP	64 LQFP	48 LQFP	System Default	GPIO	ADC /DAC	CMP	GPTM	SPI	USART /UART	I²C	SCI	N/A	I²S	N/A	N/A	SCTM /PWM	LCD	System Other
1	1	1	PA0		ADC_IN0		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL	SCI0_CLK		I2S_WS					VREF
2	2	2	PA1		ADC_IN1		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA	SCI0_DIO		I2S_BCLK					
3	3	3	PA2		ADC_IN2		GT_CH2	SPI1_MISO	USR_TX				I2S_SDO					
4	4	4	PA3		ADC_IN3		GT_CH3	SPI1_SEL	USR_RX				I2S_SDI					
5	5	5	PA4		ADC_IN4		GT_CH0	SPI0_SCK	USR_TX	I2C0_SCL	SCI1_CLK							
6	6	6	PA5		ADC_IN5		GT_CH1	SPI0_MOSI	USR_RX	I2C0_SDA	SCI1_DIO							
7	7	7	PA6		ADC_IN6		GT_CH2	SPI0_MISO	USR_RTS		SCI1_DET							
8	8	8	PA7		ADC_IN7		GT_CH3	SPI0_SEL	USR_CTS				I2S_MCLK					
9	9		PD4		ADC_IN8				UR1_TX							PWM1_CH0		
10	10		PD5		ADC_IN9				UR1_RX							PWM1_CH1		
11	11	9	PC4				GT_CH0	SPI1_SEL	USR_TX	I2C1_SCL							SEG11	
12	12	10	PC5				GT_CH1	SPI1_SCK	USR_RX	I2C1_SDA							SEG12	
13			VDD_4															
14			VSS_4															
15	13		PC8				GT_CH2	SPI1_MOSI	UR1_TX							SCTM0	SEG13	
16	14		PC9				GT_CH3	SPI1_MISO	UR1_RX							SCTM1	SEG14	
17			PD6													PWM1_CH2	SEG28	
18			PD7													PWM1_CH3	SEG29	
19	15	11	PC6						UR0_TX	I2C0_SCL								
19	15	11	USBDM															
20	16	12	USBDP															
20	16	12	PC7						UR0_RX	I2C0_SDA								
21	17	13	CLDO															
22	18	14	VDD_1															
23	19	15	VSS_1															
24	20	16	nRST															
25	21	17	VLCD															
26	22	18	X32KIN	PB10					USR_TX									
27	23	19	X32KOUT	PB11					USR_RX									
28	24	20	RTCOUT	PB12														WAKEUP
29	25		PD0							I2C0_SDA			I2S_SDI			SCTM0	SEG15	
30	26	21	XTALIN	PB13														
31	27	22	XTALOUT	PB14														

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP	64 LQFP	48 LQFP	System Default	GPIO	ADC /DAC	CMP	GPTM	SPI	USART /UART	I^{2}C	SCI	N/A	I^{2}S	N/A	N/A	SCTM /PWM	LCD	System Other
32			PD8							I2C0_SCL			I2S_BCLK				SEG30	
33			PD9							I2C0_SDA			I2S_SDO			PWM0_CH0	SEG31	
34			PD10										I2S_SDI			PWM0_CH1	SEG32	
35	28	23	PB15					SPI0_SEL	USR_TX	I2C1_SCL	SCI1_CLK		I2S_MCLK			PWM0_CH2	COM0	
36	29	24	PC0					SPI0_SCK	USR_RX	I2C1_SDA	SCI1_DIO					PWM0_CH3	COM1	
37	30		PC10				GT_CH0	SPI1_SEL					I2S_WS				SEG33/COM4	
38	31		PC11				GT_CH1	SPI1_SCK					I2S_BCLK				SEG34/COM5	
39	32		PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL			I2S_SDO			SCTM0	SEG35/COM6	
40	33		PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C0_SDA	SCI1_DET		I2S_SDI			SCTM1	SEG36/COM7	
41	34	25	PA8						USR_TX		SCI1_CLK		I2S_MCLK			PWM1_CH3	COM2	
42	35	26	PA9_BOOT					SPI0_MOSI			SCI1_DIO		I2S_WS			PWM1_CH2		CKOUT
43	36	27	PA10						USR_RX		SCI0_DET					PWM0_CH1	COM3	
44	37	28	PA11					SPI0_MISO			SCI1_DET		I2S_MCLK			SCTM0	SEG0	
45	38	29	SWCLK	PA12														
46	39	30	SWDIO	PA13														
47	40	31	PA14					SPI1_SEL	USR_RTS	I2C1_SCL	SCI0_CLK					PWM0_CH0	SEG1	
48	41	32	PA15					SPI1_SCK	USR_CTS	I2C1_SDA	SCI0_DIO					SCTM1	SEG2	
49	42	35	VDD_2															
50	43	36	VSS_2															
51	44	33	PB0					SPI1_MOSI	USR_TX	I2C0_SCL						PWM0_CH1	SEG3	
52	45	34	PB1					SPI1_MISO	USR_RX	I2C0_SDA						PWM1_CH1	SEG4	
53	46		PD1						USR_RTS		SCI0_CLK						SEG16	
54	47		PD2						USR_CTS		SCI0_DIO						SEG17	
55	48		PD3								SCI0_DET						SEG18	
56			PD11					SPI0_SCK								PWM0_CH2	SEG19	
57			PD12					SPI0_MOSI								PWM1_CH0	SEG20	
58			PD13					SPI0_MISO									SEG21	
59			PD14					SPI1_SEL								SCTM0	SEG22	
60			PD15					SPI1_SCK								SCTM1	SEG23	
61	49	37	PB2			COUT0		SPI0_SEL	UR0_TX							PWM0_CH2	SEG5	CKIN
62	50	38	PB3			COUT1		SPI0_SCK	UR0_RX							SCTM1	SEG6	

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP	64 LQFP	48 LQFP	System Default	GPIO	ADC /DAC	CMP	GPTM	SPI	USART /UART	I^2C	SCI	N/A	I^2S	N/A	N/A	SCTM /PWM	LCD	System Other
63	51	39	PB4					SPI0_MOSI	UR1_TX							SCTM0	SEG7	
64	52	40	PB5					SPI0_MISO	UR1_RX								SEG8	
65	53		PC14			COUT0				I2C0_SCL							SEG9	
66	54		PC15			COUT1				I2C0_SDA						SCTM1	SEG10	
67			PE0					SPI0_SEL			SCI0_CLK					PWM1_CH1	SEG24	
68			PE1					SPI0_SCK			SCI0_DIO					PWM0_CH3	SEG25	
69			PE2			COUT0		SPI0_MOSI									SEG26	
70	55		VDD_3															
71	56		VSS_3															
72			PE3			COUT1		SPI0_MISO					I2S_MCLK				SEG27	
73	57	41	PC1			CN0		SPI1_SEL	UR1_TX				I2S_MCLK			PWM0_CH0		
74	58	42	PC2			CP0		SPI1_SCK								PWM1_CH0		
75	59	43	PC3		DAC0_OUT	COUT0		SPI1_MOSI	UR1_RX							PWM1_CH2		
76	60	44	PB6			CN1		SPI1_MISO	UR0_TX		SCI1_CLK		I2S_BCLK					
77	61	45	PB7			CP1				I2C1_SCL	SCI1_DET		I2S_SDO			PWM0_CH3		
78	62	46	PB8		DAC1_OUT	COUT1			UR0_RX	I2C1_SDA	SCI1_DIO		I2S_SDI			PWM1_CH3		
79	63	47	VDDA															
80	64	48	VSSA															

Table 5. HT32F57331/HT32F57341 Pin Description

Pin Number		Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
64 LQFP	48 LQFP					Default Function (AF0)
1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9		PD4	AI/O	33V	4/8/12/16 mA	PD4
10		PD5	AI/O	33V	4/8/12/16 mA	PD5
11	9	PC4	I/O	33V	4/8/12/16 mA	PC4
12	10	PC5	I/O	33V	4/8/12/16 mA	PC5
13		PC8	I/O	33V	4/8/12/16 mA	PC8
14		PC9	I/O	33V	4/8/12/16 mA	PC9
15	11	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	USBDM[(4)]	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	USBDP[(4)]	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
18	14	VDD_1	P	—	—	Voltage for digital I/O
19	15	VSS_1	P	—	—	Ground reference for digital I/O
20	16	nRST[(3)]	I (V_{DD})	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode.
21	17	VLCD	P	—	—	Voltage for LCD power supply It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1 for LCD supply power with internal charge pump mode, or connected a general bypass capacitor for external LCD supply power.
22	18	PB10[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
23	19	PB11[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
24	20	PB12[(3)]	I/O (V_{DD})	33V	4/8/12/16 mA	RTCOUT
25		PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23	PB15	I/O	33V	4/8/12/16 mA	PB15
29	24	PC0	I/O	33V	4/8/12/16 mA	PC0

Pin Number		Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
64 LQFP	48 LQFP					Default Function (AF0)
30		PC10	I/O	33V	4/8/12/16 mA	PC10
31		PC11	I/O	33V	4/8/12/16 mA	PC11
32		PC12	I/O	33V	4/8/12/16 mA	PC12
33		PC13	I/O	33V	4/8/12/16 mA	PC13
34	25	PA8	I/O	33V	4/8/12/16 mA	PA8
35	26	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
36	27	PA10	I/O	33V	4/8/12/16 mA	PA10
37	28	PA11	I/O	33V	4/8/12/16 mA	PA11
38	29	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	30	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	31	PA14	I/O	33V	4/8/12/16 mA	PA14
41	32	PA15	I/O	33V	4/8/12/16 mA	PA15
42	35	VDD_2	P	—	—	Voltage for digital I/O
43	36	VSS_2	P	—	—	Ground reference for digital I/O
44	33	PB0	I/O	33V	4/8/12/16 mA	PB0
45	34	PB1	I/O	33V	4/8/12/16 mA	PB1
46		PD1	I/O	33V	4/8/12/16 mA	PD1
47		PD2	I/O	33V	4/8/12/16 mA	PD2
48		PD3	I/O	33V	4/8/12/16 mA	PD3
49	37	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	PB5	I/O	33V	4/8/12/16 mA	PB5
53		PC14	I/O	33V	4/8/12/16 mA	PC14
54		PC15	I/O	33V	4/8/12/16 mA	PC15
55		VDD_3	P	—	—	Voltage for digital I/O
56		VSS_3	P	—	—	Ground reference for digital I/O
57	41	PC1	I/O	33V	4/8/12/16 mA	PC1
58	42	PC2	I/O	33V	4/8/12/16 mA	PC2
59	43	PC3	I/O	33V	4/8/12/16 mA	PC3
60	44	PB6	I/O	33V	4/8/12/16 mA	PB6
61	45	PB7	I/O	33V	4/8/12/16 mA	PB7
62	46	PB8	I/O	33V	4/8/12/16 mA	PB8
63	47	VDDA	P	—	—	Analog voltage for ADC
64	48	VSSA	P	—	—	Ground reference for ADC

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 33V = 3.3 V tolerant, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the USB interface can be used for communication.

Table 6. HT32F57342/HT32F57352 Pin Description

Pin Number			Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
80 LQFP	64 LQFP	48 LQFP					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9	9		PD4	AI/O	33V	4/8/12/16 mA	PD4
10	10		PD5	AI/O	33V	4/8/12/16 mA	PD5
11	11	9	PC4	I/O	33V	4/8/12/16 mA	PC4
12	12	10	PC5	I/O	33V	4/8/12/16 mA	PC5
13			VDD_4	P	—	—	Voltage for digital I/O
14			VSS_4	P	—	—	Ground reference for digital I/O
15	13		PC8	I/O	33V	4/8/12/16 mA	PC8
16	14		PC9	I/O	33V	4/8/12/16 mA	PC9
17			PD6	I/O	33V	4/8/12/16 mA	PD6
18			PD7	I/O	33V	4/8/12/16 mA	PD7
19	15	11	PC6	I/O	33V	4/8/12/16 mA	PC6
19	15	11	USBDM[(4)]	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
20	16	12	USBDP[(4)]	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
20	16	12	PC7	I/O	33V	4/8/12/16 mA	PC7
21	17	13	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
22	18	14	VDD_1	P	—	—	Voltage for digital I/O
23	19	15	VSS_1	P	—	—	Ground reference for digital I/O
24	20	16	nRST[(3)]	I (V_{DD})	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode.
25	21	17	VLCD	P	—	—	Voltage for LCD power supply It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1 for LCD supply power with internal charge pump mode, or connected a general bypass capacitor for external LCD supply power.
26	22	18	PB10[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
27	23	19	PB11[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
28	24	20	PB12[(3)]	I/O (V_{DD})	33V	4/8/12/16 mA	RTCOUT
29	25		PD0	I/O	33V	4/8/12/16 mA	PD0

Pin Number			Pin Name	Type[1]	I/O Structure[2]	Output Driving	Description
80 LQFP	64 LQFP	48 LQFP					Default Function (AF0)
30	26	21	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
31	27	22	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
32			PD8	I/O	33V	4/8/12/16 mA	PD8
33			PD9	I/O	33V	4/8/12/16 mA	PD9
34			PD10	I/O	33V	4/8/12/16 mA	PD10
35	28	23	PB15	I/O	33V	4/8/12/16 mA	PB15
36	29	24	PC0	I/O	33V	4/8/12/16 mA	PC0
37	30		PC10	I/O	33V	4/8/12/16 mA	PC10
38	31		PC11	I/O	33V	4/8/12/16 mA	PC11
39	32		PC12	I/O	33V	4/8/12/16 mA	PC12
40	33		PC13	I/O	33V	4/8/12/16 mA	PC13
41	34	25	PA8	I/O	33V	4/8/12/16 mA	PA8
42	35	26	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
43	36	27	PA10	I/O	33V	4/8/12/16 mA	PA10
44	37	28	PA11	I/O	33V	4/8/12/16 mA	PA11
45	38	29	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
46	39	30	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
47	40	31	PA14	I/O	33V	4/8/12/16 mA	PA14
48	41	32	PA15	I/O	33V	4/8/12/16 mA	PA15
49	42	35	VDD_2	P	—	—	Voltage for digital I/O
50	43	36	VSS_2	P	—	—	Ground reference for digital I/O
51	44	33	PB0	I/O	33V	4/8/12/16 mA	PB0
52	45	34	PB1	I/O	33V	4/8/12/16 mA	PB1
53	46		PD1	I/O	33V	4/8/12/16 mA	PD1
54	47		PD2	I/O	33V	4/8/12/16 mA	PD2
55	48		PD3	I/O	33V	4/8/12/16 mA	PD3
56			PD11	I/O	33V	4/8/12/16 mA	PD11
57			PD12	I/O	33V	4/8/12/16 mA	PD12
58			PD13	I/O	33V	4/8/12/16 mA	PD13
59			PD14	I/O	33V	4/8/12/16 mA	PD14
60			PD15	I/O	33V	4/8/12/16 mA	PD15
61	49	37	PB2	I/O	33V	4/8/12/16 mA	PB2
62	50	38	PB3	I/O	33V	4/8/12/16 mA	PB3
63	51	39	PB4	I/O	33V	4/8/12/16 mA	PB4
64	52	40	PB5	I/O	33V	4/8/12/16 mA	PB5
65	53		PC14	I/O	33V	4/8/12/16 mA	PC14
66	54		PC15	I/O	33V	4/8/12/16 mA	PC15
67			PE0	I/O	33V	4/8/12/16 mA	PE0
68			PE1	I/O	33V	4/8/12/16 mA	PE1
69			PE2	I/O	33V	4/8/12/16 mA	PE2
70	55		VDD_3	P	—	—	Voltage for digital I/O

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
80 LQFP	64 LQFP	48 LQFP					Default Function (AF0)
71	56		VSS_3	P	—	—	Ground reference for digital I/O
72			PE3	I/O	33V	4/8/12/16 mA	PE3
73	57	41	PC1	AI/O	33V	4/8/12/16 mA	PC1
74	58	42	PC2	AI/O	33V	4/8/12/16 mA	PC2
75	59	43	PC3	AI/O	33V	4/8/12/16 mA	PC3
76	60	44	PB6	AI/O	33V	4/8/12/16 mA	PB6
77	61	45	PB7	AI/O	33V	4/8/12/16 mA	PB7
78	62	46	PB8	AI/O	33V	4/8/12/16 mA	PB8
79	63	47	VDDA	P	—	—	Analog voltage for ADC and Comparators
80	64	48	VSSA	P	—	—	Ground reference for ADC and Comparators

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 33V = 3.3 V tolerant, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the USB interface can be used for communication.

5 Electrical Characteristics

Power Supply Scheme

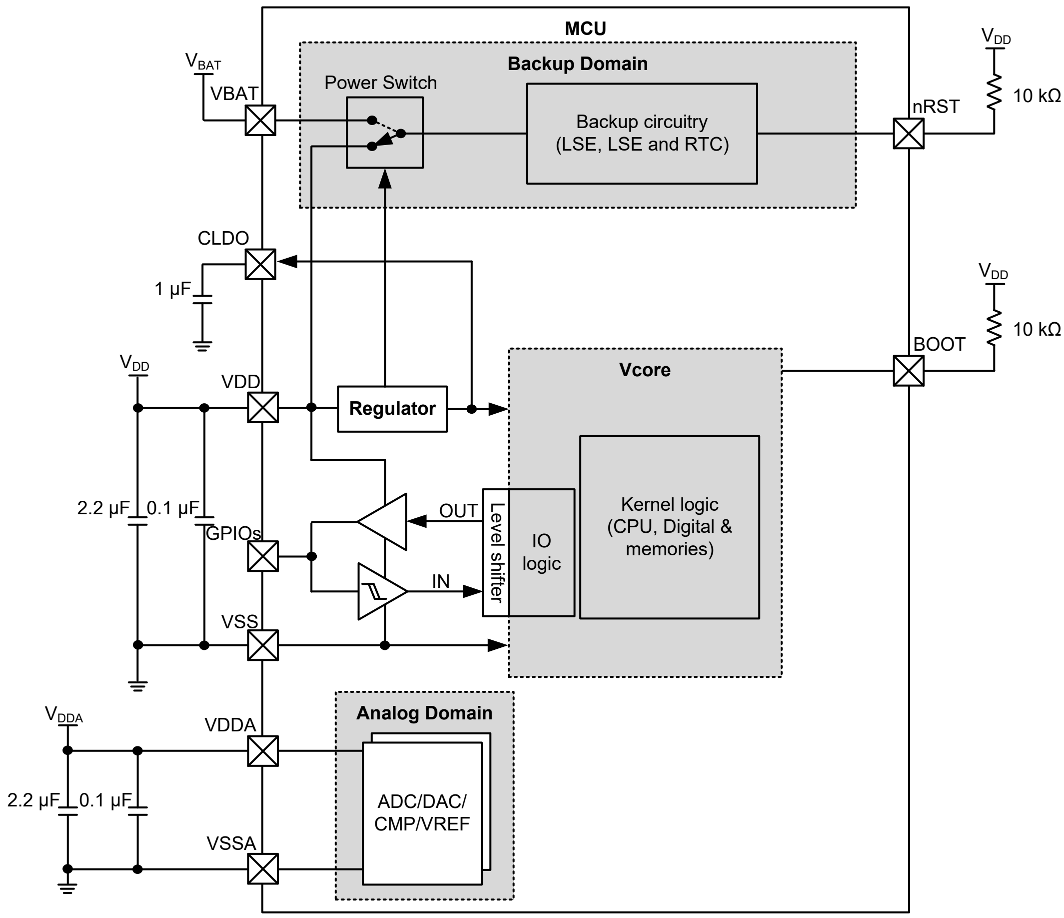


Figure 9. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the BOOT pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{LCD}	LCD Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 8. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	1.65	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V
V_{LCD}	LCD Operating Voltage	—	2.2	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 9. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 10 mA and voltage variant = ± 5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
		V_{DD} = 1.65 V ~ 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	20	25	
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	µF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 10. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{ULDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	µF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state
- All peripherals are disabled unless specifically stated otherwise
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}

Table 11. HT32F57331/HT32F57341 Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A 25 °C	Max. @ T_A 85 °C	Unit
I_{DD}	Run Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz	All peripherals enabled	14.9	17.0	—	mA
				All peripherals disabled	6.9	7.9	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz	All peripherals enabled	11.9	13.6	—	
				All peripherals disabled	6.5	7.4	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz	All peripherals enabled	6.2	7.1	—	
				All peripherals disabled	3.2	3.6	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	3.2	3.6	—	
				All peripherals disabled	1.4	1.6	—	
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	13.2	17.5	—	µA
				All peripherals disabled	9.2	12.2	—	
	Sleep Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, MCU core sleep	All peripherals enabled	10.3	11.8	—	mA
				All peripherals disabled	1.5	1.7	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, MCU core sleep	All peripherals enabled	7.1	8.1	—	
				All peripherals disabled	1.2	1.3	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, MCU core sleep	All peripherals enabled	4.2	4.8	—	
				All peripherals disabled	0.9	1.0	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, MCU core sleep	All peripherals enabled	2.4	2.7	—	
				All peripherals disabled	0.4	0.5	—	

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A 25 °C	Max. @ T_A 85 °C	Unit
I_{DD}	Deep-Sleep1 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	5.0	7.6	—	µA
	Deep-Sleep2 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	5.0	7.6	—	µA
			V_{DD} = V_{LCD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on, LCD ON(5), external V_{LCD} = V_{DD}	7.5	—	—	
			V_{DD} = 2.7 V, V_{LCD} = 3.25 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC off, LCD on(6), internal V_{LCD} pump	55.3	—	—	
	Power-Down Mode	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on	1.40	2.15	—	µA
			V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off	1.30	1.95	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.
6. LCD enabled with internal V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

Table 12. HT32F57342/HT32F57352 Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A 25 °C	Max. @ T_A 85 °C	Unit
I_{DD}	Run Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 60 MHz	All peripherals enabled	20.0	22.8	—	mA
				All peripherals disabled	8.6	9.8	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	15.8	18.0	—	
				All peripherals disabled	7.9	9.1	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	8.3	9.5	—	
				All peripherals disabled	3.9	4.4	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 48 MHz	All peripherals enabled	4.2	4.8	—	
				All peripherals disabled	1.6	1.9	—	
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz LDO off, ULDO on	All peripherals enabled	17.3	24.5	—	µA
				All peripherals disabled	11.1	17.1	—	
	Sleep Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 60 MHz, MCU core sleep	All peripherals enabled	14.7	16.9	—	mA
				All peripherals disabled	2.1	2.4	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 40 MHz, MCU core sleep	All peripherals enabled	10.2	11.6	—	
				All peripherals disabled	1.6	1.8	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 40 MHz, MCU core sleep	All peripherals enabled	5.9	6.7	—	
				All peripherals disabled	1.1	1.3	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz PLL = 48 MHz, MCU core sleep	All peripherals enabled	3.2	3.6	—	
				All peripherals disabled	0.5	0.6	—	

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2">Parameter</th><th rowspan="2">f_{HCLK}</th><th rowspan="2">Conditions</th><th rowspan="2">Typ.</th><th colspan="2">Max. @ T_A</th><th rowspan="2">Unit</th></tr>
<tr><th>25 °C</th><th>85 °C</th></tr>
<tr><td rowspan="7">I_{DD}</td><td>Deep-Sleep1 Mode</td><td>—</td><td>V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on</td><td>5.7</td><td>11.3</td><td>—</td><td rowspan="7">μA</td></tr>
<tr><td rowspan="3">Deep-Sleep2 Mode</td><td rowspan="3">—</td><td>V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on</td><td>5.7</td><td>11.3</td><td>—</td></tr>
<tr><td>V_{DD} = V_{LCD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on, LCD ON(5), external V_{LCD} = V_{DD}</td><td>8.2</td><td>—</td><td>—</td></tr>
<tr><td>V_{DD} = 2.7 V, V_{LCD} = 3.25 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC off, LCD on(6), internal V_{LCD} pump</td><td>56.0</td><td>—</td><td>—</td></tr>
<tr><td rowspan="2">Power-Down Mode</td><td rowspan="2">—</td><td>V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on</td><td>1.35</td><td>2.05</td><td>—</td></tr>
<tr><td>V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off</td><td>1.30</td><td>2.00</td><td>—</td></tr>
</table>

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.
6. LCD enabled with internal V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

Reset and Supply Monitor Characteristics

Table 13. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.4	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 14. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	200	—	μs
I_{DDLVD}	Operation Current [(2)]	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 15. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0 V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1	—	—	160	Ω
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 16. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 1.65 V ~ 2.7 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 17. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	1.65	—	3.6	V
f_{CK_HSI}	HSI Frequency	V_{DD} = 3.3 V	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 1.65 V ~ 3.6 V, T_A = -20 °C ~ 60 °C	-2.5	—	2.5	%
		V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{CK_HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{CK_HSI} = 8 MHz	—	300	500	μA
	HSI Oscillator Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{CK_HSI} = 8 MHz	—	—	10	μs

Table 18. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V	—	—	100	μs

System PLL Characteristics

Table 19. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

USB PLL Characteristics

Table 20. USB PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	USB PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	USB PLL Output Clock	—	64	—	96	MHz
t_{LOCK}	USB PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 21. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 22. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	$V_I = V_{SS}$, On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	3.3 V I/O	$V_I = V_{DD}$, On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	3.3 V I/O		-0.4	—	V_{DD} × 0.35	V
		Reset pin		-0.4	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.4	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.4	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		16	—	—	
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ
C_{IO}	I/O Pin Capacitance	—		—	4.2	—	pF

ADC Characteristics

Table 23. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	A/D Converter Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

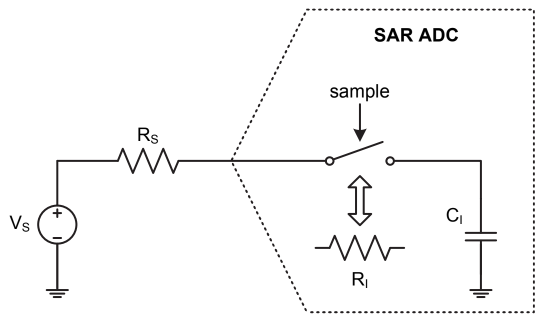


Figure 10. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 24. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		1.65	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 ˚C Temperature	V_{DDA} ≥ 1.65 V	VREFSEL[1:0] = 00	1.190	1.215	1.240	V
		V_{DDA} ≥ 2.30 V	VREFSEL[1:0] = 01	1.96	2.00	2.04	
		V_{DDA} ≥ 2.80 V	VREFSEL[1:0] = 10	2.45	2.50	2.55	
		V_{DDA} ≥ 3.00 V	VREFSEL[1:0] = 11	2.65	2.70	2.75	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 1.65 V ~ 3.6 V, V_{REF} = 1.215 V, T_A = -40 °C ~ 85 °C		-3.0	—	+3.0	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	45	55	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

V_{DDA} Monitor Characteristics

Table 25. V_{DDA} Monitor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R	Resistor Bridge for V_{DDA}	—	—	50	—	kΩ
Q	Ratio on V_{DDA} Measurement	—	—	2	—	—
E_R	Error on Ratio	—	-1	—	+1	%
t_{SVDDA}	ADC Sampling Time when Reading the V_{DDA}	—	5	—	—	μs

Note: Data based on characterization results only, not tested in production.

Comparator Characteristics

Table 26. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	Comparator mode		2.0	3.3	3.6	V
V_{IN}	Input Common Mode Voltage Range	CP or CN		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage(1)	T_A = 25 °C		-15	—	15	mV
V_{HYS}	Input Hysteresis V_{DDA} = 3.3 V	No hysteresis, CMPHM [1:0] = 00		—	0	—	mV
		Low hysteresis, CMPHM [1:0] = 01		—	30	—	mV
		Middle hysteresis, CMPHM [1:0] = 10		—	70	—	mV
		High hysteresis, CMPHM [1:0] = 11		—	100	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode	V_{DDA} ≥ 2.7 V	—	50	100	ns
			V_{DDA} < 2.7 V	—	100	250	ns
		Low Speed Mode		—	2	5	µs
I_{CMP}	Current Consumption V_{DDA} = 3.3 V	High Speed Mode		—	180	—	µA
		Low Speed Mode		—	30	—	µA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid		—	—	50	µs
I_{CMP_DN}	Comparator Power Down Supply Current	CMPEN = 0, CVREN = 0, CVROE = 0		—	—	0.1	µA
Comparator Voltage Reference (CVR)							
V_{CVR}	Output Range	—		V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—		—	8	—	bits
t_{CVRST}	Setting Time	V_{DDA} = 3.3V, CVROE = 1, C_{LOAD} ≤ 100 pF; R_{LOAD} ≥ 50 kΩ CVR Scaler Setting Time from CVRVAL = "00000000" to "11111111"		—	—	100	µs
I_{CVR}	Current Consumption V_{DDA} = 3.3 V	CVREN = 1, CVROE = 0		—	65	—	µA
		CVREN = 1, CVROE = 1		—	80	110	µA

Note: Data based on characterization results only, not tested in production.

DAC Characteristics

Table 27. DAC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog Supply Voltage	T_A = -40 °C ~ 85 °C	2.5	—	3.6	V
V_{DACREF}	Reference Supply Voltage	—	2.0	—	V_{DDA}	V
V_{SSA}	Ground	—	0	—	0	V
R_L	Resistive Load With Buffer	—	50	—	—	kΩ
C_L	Capacitive Load	—	—	—	50	pF
$DACOUT_{MIN}$	Lowest DACOUT Voltage with Buffer	—	0.2	—	—	V
$DACOUT_{MAX}$	Highest DACOUT Voltage with Buffer	V_{DACREF} = V_{DDA}	—	—	V_{DACREF} - 0.2	V
		V_{DACREF} = V_{REF}	—	—	V_{DACREF}	V
I_{DD}	DAC DC Current Consumption in Quiescent Mode (in V_{DDA} + V_{REF})	With no load, highest code (0xFFFH) on the input @ V_{DDA} = 3.6V	—	—	1	mA
I_{DDPWD}	DAC DC Current Consumption in Power Down Mode (in V_{DDA} + V_{REF})	With no load	—	—	1	nA
DNL	Differential Non-linearity (Difference between two consecutive code – 1 LSB)	DAC in 10-bit configuration (B1 = B0 = 0 always)	—	—	±1	LSB
INL	Integral Non-linearity (Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	DAC in 10-bit configuration (B1 = B0 = 0 always)	—	—	±2	LSB
E_O	Offset Error (Difference between measured value at Code (0x800H) and the ideal value = V_{REF} / 2)	DAC in 10-bit configuration (B1 = B0 = 0 always) @ V_{REF} = 3.6V	—	±10	—	mV
E_G	Gain Error	—	—	±0.5	—	%
t_{SETTLE}	Settling Time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DACOUT reaches final value ±1 LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 50 kΩ	—	—	5	μs
SR_{DAC}	Max frequency for a correct DACOUT change when small variation in the input code (from code i to i + 1 LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 50 kΩ	—	—	0.33	MS/s

Note: Data based on characterization results only, not tested in production.

GPTM/PWM/SCTM Characteristics

Table 28. GPTM/PWM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM, PWM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 29. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL And SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL And SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

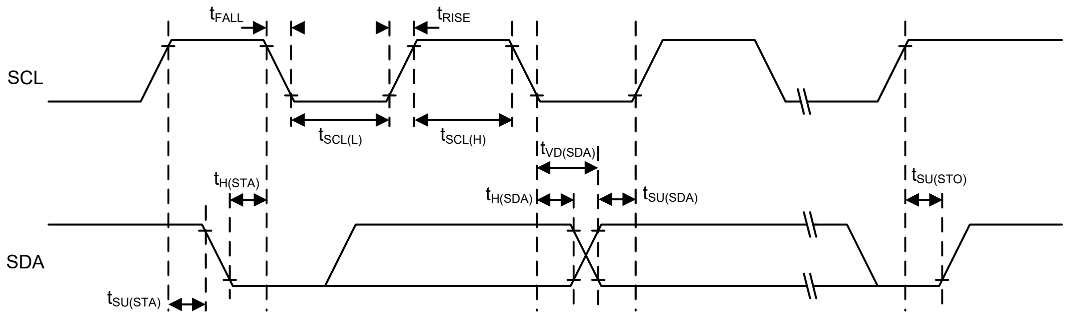


Figure 11. I²C Timing Diagrams

SPI Characteristics

Table 30. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

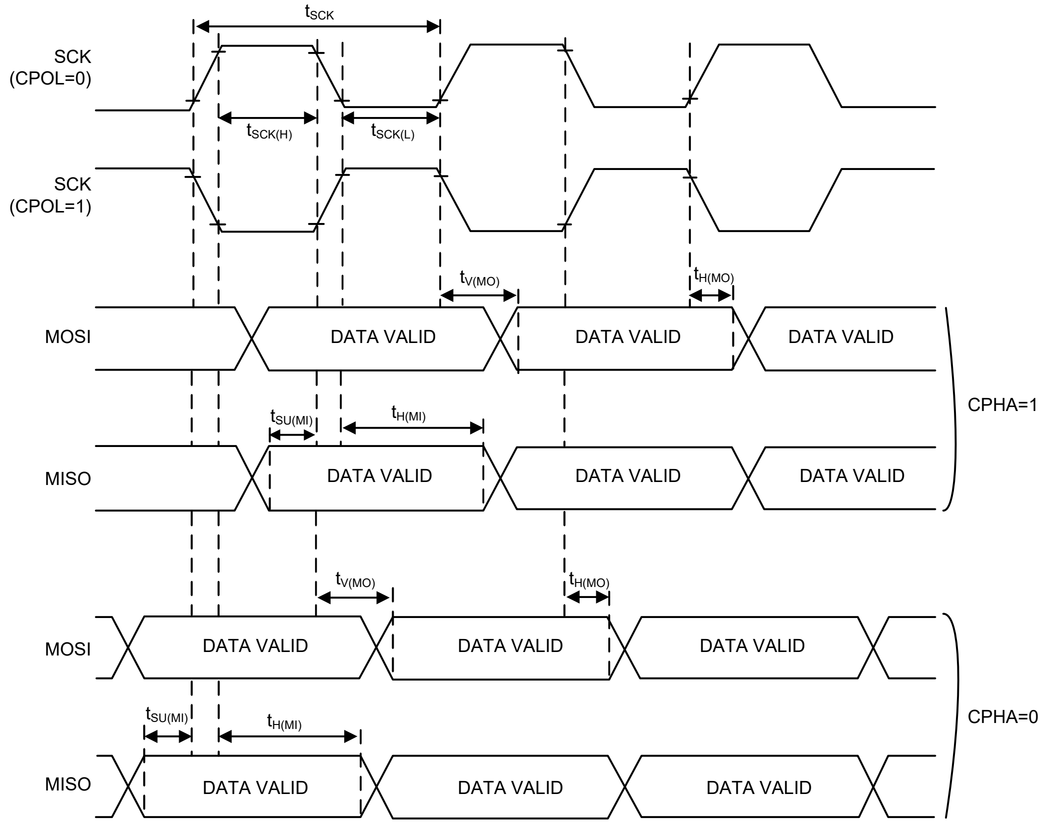


Figure 12. SPI Timing Diagram – SPI Master Mode

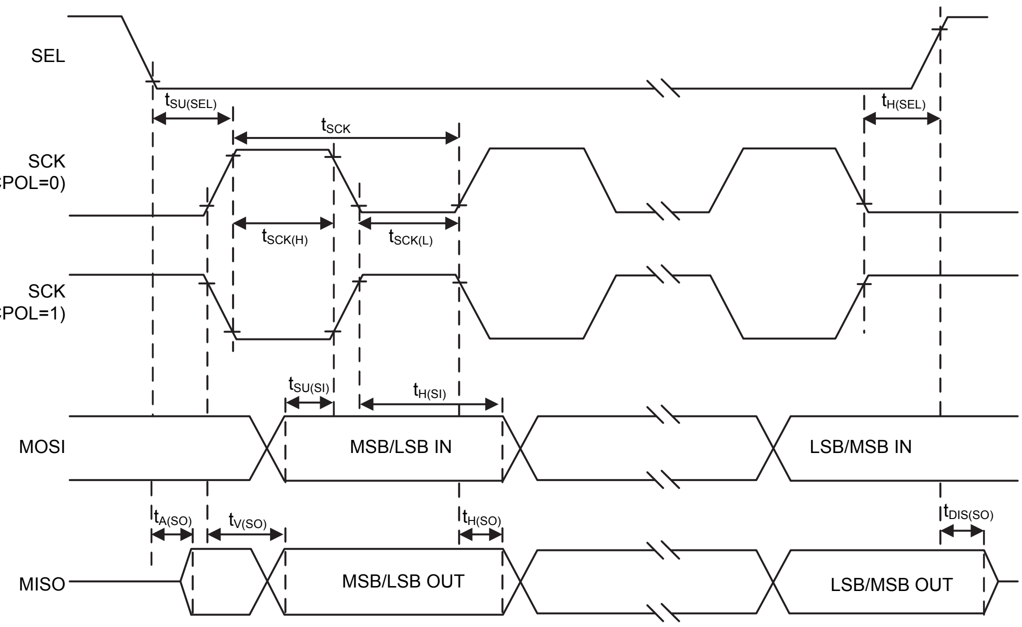


Figure 13. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

I²S Characteristics

Table 31. I²S Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I²S Master Mode						
$t_{WSD(MO)}$	WS Output to BCLK Delay	—	—	TBD	—	ns
$t_{DOD(MO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(MI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(MI)}$	Data Input Hold Time	—	—	TBD	—	ns
I²S Slave Mode						
$t_{BCH(SI)}$	BCLK High Pulse Width	—	—	TBD	—	ns
$t_{BCL(SI)}$	BCLK Low Pulse Width	—	—	TBD	—	ns
$t_{WSS(SI)}$	WS Input Setup Time	—	—	TBD	—	ns
$t_{DOD(SO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(SI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(SI)}$	Data Input Hold Time	—	—	TBD	—	ns

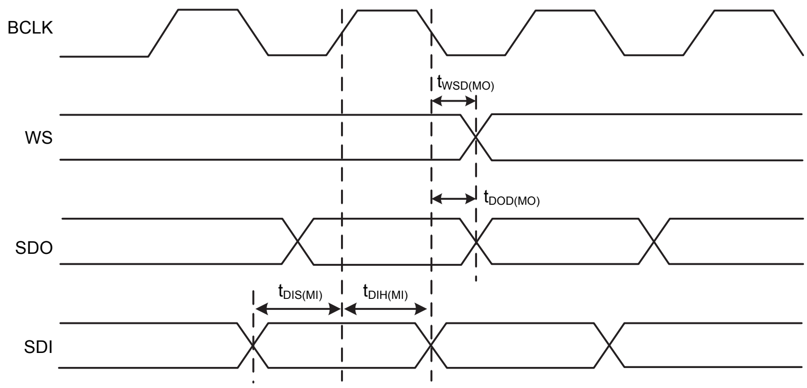


Figure 14. I²S Master Mode Timing Diagram

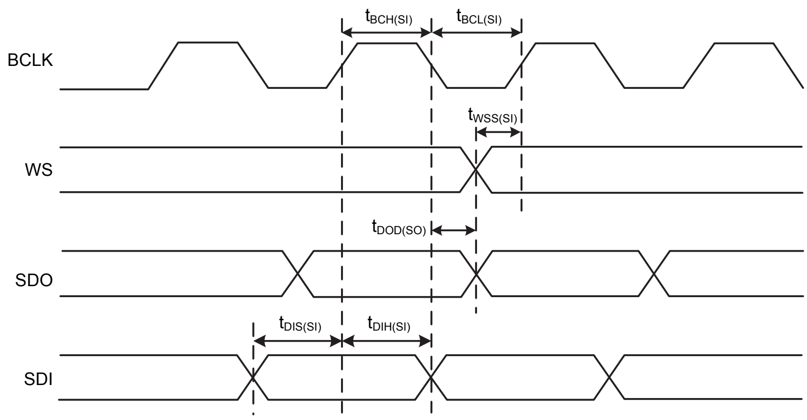


Figure 15. I²S Slave Mode Timing Diagram

LCD Characteristics

Table 32. LCD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LCD}	LCD External Voltage	—	—	—	3.6	V
	LCD Internal Charge Pump Voltage	CPVS = 000	—	2.65	—	V
		CPVS = 001	—	2.75	—	V
		CPVS = 010	—	2.85	—	V
		CPVS = 011	—	2.95	—	V
		CPVS = 100	—	3.1	—	V
		CPVS = 101	—	3.25	—	V
		CPVS = 110	—	3.4	—	V
		CPVS = 111	—	3.55	3.6	V
C_{LCD}	V_{LCD} External Capacitor	—	0.22	—	2.2	µF
I_{LCD}	Supply Current @ V_{DD} = 3.3 V	External V_{LCD} (1)	—	2.4	—	µA
	Supply Current @ V_{DD} = 2.7 V	Internal charge pump (2)	—	50	—	
R_H	Internal Low Drive Resister Network Overall Value	—	—	3	—	MΩ
R_L	Internal High Drive Resister Network Overall Value	—	—	120	—	kΩ
V_{44}	Segment/Common Highest Level Voltage	—	—	—	V_{LCD}	V
V_{34}	Segment/Common 3/4 Level Voltage	—	—	3/4 V_{LCD}	—	V
V_{23}	Segment/Common 2/3 Level Voltage	—	—	2/3 V_{LCD}	—	V
V_{12}	Segment/Common 1/2 Level Voltage	—	—	1/2 V_{LCD}	—	V
V_{13}	Segment/Common 1/3 Level Voltage	—	—	1/3 V_{LCD}	—	V
V_{14}	Segment/Common 1/4 Level Voltage	—	—	1/4 V_{LCD}	—	V
V_0	Segment/Common Lowest Level Voltage	—	0	—	—	V

Note: 1. LCD enabled with external V_{LCD} = V_{DD} = 3.3 V, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

2. LCD enabled with internal charge pump V_{LCD} = 3.25 V, V_{DD} = 2.7 V, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

3. Data based on characterization results only, not tested in production.

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 33. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	1.5 kΩ R_L to V_{DD33}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.
2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the V_{DD} voltage range of 2.7 to 3.0 V.
3. R_L is the resistor load connected to the USB driver USBDP.

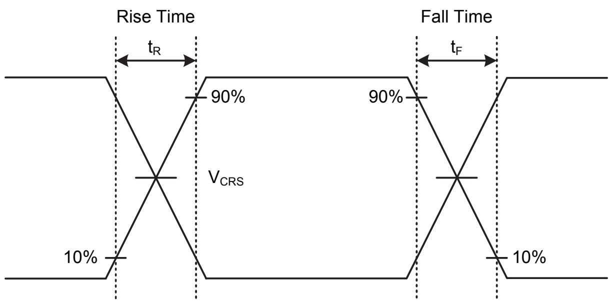


Figure 16. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 34. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Time	C_L = 50 pF	4	—	20	ns
t_F	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{R/F}$	Rise Time / Fall Time Matching	$t_{R/F} = t_R / t_F$	90	—	110	%

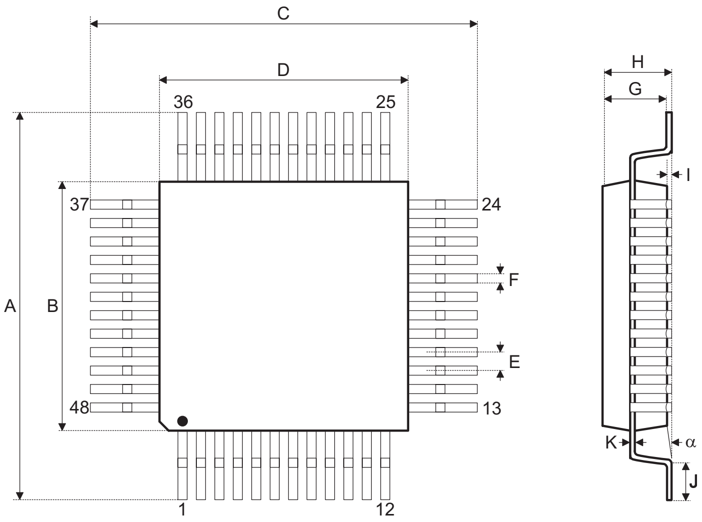
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

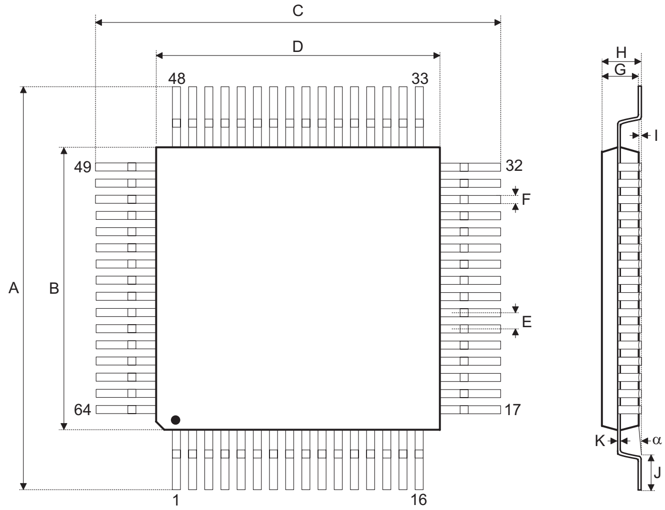
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

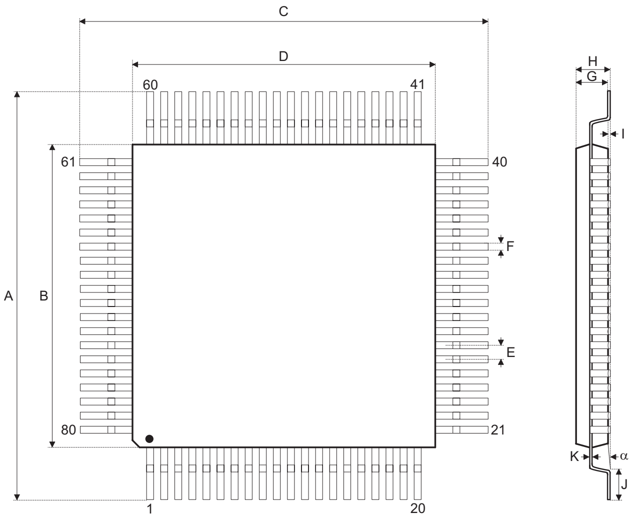
64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm × 10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.016 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12 BSC	—
B	—	10 BSC	—
C	—	12 BSC	—
D	—	10 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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