

HT32F12365/12366/22366

Series Datasheet

32-bit ARM[®] Cortex[™] M3 Microcontroller,
up to 256 KB Flash and 128 KB SRAM with 2 MSPS ADC, USART, UART, SPI, I²C, I²S, MCTM, GPTM,
BFTM, PDMA, SCI, CRC, RTC, WDT, AES, EBI, CSIF and USB2.0 FS

Contents

1	General Description.....	6
2	Features	7
2.1	Core	7
2.2	On-chip Memory	7
2.3	Flash Memory Controller - FMC.....	7
2.4	Reset Control Unit - RSTCU.....	8
2.5	Clock Control Unit - CKCU.....	8
2.6	Power Management - PWRCU.....	9
2.7	External Interrupt/Event Controller - EXTI	9
2.8	Analog to Digital Converter - ADC	9
2.9	Analog Comparator - CMP	10
2.10	I/O Ports - GPIO.....	10
2.11	Motor Control Timer - MCTM.....	11
2.12	PWM Generation and Capture Timers - GPTM.....	11
2.13	Basic Function Timer - BFTM.....	12
2.14	Watchdog Timer - WDT	12
2.15	Real Time Clock - RTC	12
2.16	Inter-integrated Circuit - I2C.....	13
2.17	Serial Peripheral Interface - SPI.....	13
2.18	Universal Synchronous Asynchronous Receiver Transmitter - USART	14
2.19	Universal Asynchronous Receiver Transmitter - UART	15
2.20	Smart Card Interface - SCI	15
2.21	Inter-IC Sound – I2S.....	16
2.22	Cyclic Redundancy Check - CRC.....	16
2.23	Peripheral Direct Memory Access - PDMA	17
2.24	External Bus Interface - EBI	17
2.25	Universal Serial Bus Device Controller - USB	17
2.26	CMOS Sensor Interface - CSIF (HT32F22366 only).....	18
2.27	Advanced Encryption Standard - AES	18
2.28	Secure Digital Input Output - SDIO	19
2.29	Debug Support.....	19
2.30	Package and Operation Temperature.....	19
3	Overview.....	20
3.1	Device Information	20
3.2	Block Diagram.....	21
3.3	Memory Map	22

3.4	Clock Structure	25
4	Pin Assignment.....	26
5	Electrical Characteristics	36
5.1	Absolute Maximum Ratings	36
5.2	Recommended DC Operating Conditions.....	36
5.3	On-Chip LDO Voltage Regulator Characteristics	37
5.4	Power Consumption.....	37
5.5	Reset and Supply Monitor Characteristics.....	37
5.6	External Clock Characteristics	38
5.7	Internal Clock Characteristics	39
5.8	PLL Characteristics	40
5.9	Memory Characteristics.....	40
5.10	I/O Port Characteristics	40
5.11	ADC Characteristics	42
5.12	Comparator Characteristics	43
5.13	GPTM/MCTM Characteristics	44
5.14	I ² C Characteristics	44
5.15	SPI Characteristics	45
5.16	I ² S Characteristics.....	46
5.17	USB Characteristics	47

Confidential

List of tables

Table 1 HT32F12365/12366/22366 Features and Peripheral List	20
Table 2 HT32F12365/12366/22366 Register Map.....	23
Table 3 HT32F12365/12366/22366 Series Pin Assignment for LQFP 64 / 48 Package	29
Table 4 HT32F12365/12366/22366 Pin Description	33
Table 5 Absolute Maximum Ratings	36
Table 6 Recommended DC Operating Conditions	36
Table 7 LDO Characteristics	37
Table 8 Power Consumption Characteristics	37
Table 9 V _{DD} Power Reset Characteristics	37
Table 10 LVD/BOD Characteristics	38
Table 11 High Speed External Clock (HSE) Characteristics	38
Table 12 Low Speed External Clock (LSE) Characteristics	39
Table 13 High Speed Internal Clock (HSI) Characteristics	39
Table 14 Low Speed Internal Clock (LSI) Characteristics	40
Table 15 PLL Characteristics	40
Table 16 Flash Memory Characteristics	40
Table 17 I/O Port Characteristics	40
Table 18 ADC Characteristics	42
Table 19 Comparator Characteristics	43
Table 20 SCTM/GPTM/MCTM Characteristics	44
Table 21 I ² C Characteristics	44
Table 22 SPI Characteristics	錯誤! 尚未定義書籤。
Table 23 I ² S Characteristics	46
Table 24 USB DC Electrical Characteristics	47
Table 25 USB AC Electrical Characteristics	48

List of figures

Figure 1 HT32F12365/12366/22366 Block Diagram	21
Figure 2 HT32F12365/12366/22366 Memory Map.....	22
Figure 3 HT32F12365/12366/22366 Clock Structure.....	25
Figure 4 HT32F12365/12366/22366 LQFP-48 Pin Assignment	26
Figure 5 HT32F12365/12366/22366 LQFP-64 Pin Assignment	27
Figure 7 HT32F12365/12366/22366 LQFP-100 Pin Assignment.....	28
Figure 6 ADC Sampling Network Model.....	42
Figure 7 I ² C Timing Diagrams	44
Figure 8 SPI Timing Diagrams - SPI Master Mode.....	45
Figure 9 SPI Timing Diagrams - SPI Slave Mode with CPHA=1	46
Figure 10 Timing of I ² S Master Mode	47
Figure 11 Timing of I ² S Slave Mode.....	47
Figure 12 USB Signal Rise Time and Fall Time and Cross-Point Voltage (VCRS) Definition.....	48

Confidential

1 General Description

The Holtek HT32F12365/12366/22366 devices are high performance, low power consumption 32-bit microcontrollers based around an ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and includes advanced debug support.

The devices operate at a frequency of up to 96 MHz with a Flash accelerator to obtain maximum efficiency. They provide up to 256 KB of embedded Flash memory for code/data storage and 128 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, UART, SPI, I²S, PDMA, GPTM, MCTM, SCI, EBI, CRC-16/32, AES-128/256, USB2.0 FS and CSIF SWJ-DP (Serial Wire and JTAG Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.

2 Features

2.1 Core

- 32-bit ARM® Cortex™-M3 processor core
- Up to 96 MHz operating frequency
- 1.25 DMIPS/MHz (Dhrystone 2.1)
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many special features such as a Thumb-2 instruction set, hardware divider, low latency interrupt response time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets.

2.2 On-chip Memory

- Up to 256 KB on-chip Flash memory for instruction/data and option storage
- Up to 128 KB on-chip SRAM
- Supports multiple boot modes

The ARM® Cortex™-M3 processor is structured using Harvard architecture which uses a separate bus structure to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4 GB due to its 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation for different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F12365/12366/22366 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

2.3 Flash Memory Controller - FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

2.4 Reset Control Unit - RSTCU

- Supply supervisor:
 - Power On Reset / Power Down Reset – POR/PDR
 - Brown-out Detector - BOD
 - Programmable Low Voltage Detector - LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

2.5 Clock Control Unit - CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8MHz RC oscillator trimmed to $\pm 2\%$ accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be

up to 96 MHz.

2.6 Power Management - PWRCU

- Single V_{DD} power supply : 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- VBAT battery power supply for RTC and backup registers
- Three power domains: V_{DD} , 1.5 V and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

2.7 External Interrupt/Event Controller - EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

2.8 Analog to Digital Converter - ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 16 external analog input channels
- Conversion range: $V_{REF+} \sim V_{REF-}$

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels,

which include 16 external analog signal channels and 2 internal channels can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

2.9 Analog Comparator - CMP

- Two rail-to-rail comparator
- Each comparator has configurable negative inputs used for flexible voltage selection
- Dedicated I/O pin or internal voltage reference provided by 6-bit scaler.
- Programmable hysteresis
- Programming speed and consumption
- Comparator output can be output to I/O or to timers or ADC trigger inputs
- 6-bit scaler can be configurable to dedicated I/O for voltage reference.
- Comparator has interrupt generation capability with wakeup from Sleep or Deep Sleep modes through the EXTI controller.

The two general purpose comparators (CMP) are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or wakeup the MCU Deep Sleep mode through EXTI wakeup event management unit.

2.10 I/O Ports - GPIO

- Up to 80 GPIOs
- Port A, B, C, D, E are mapped as 16 external interrupts - EXTI
- Almost I/O pins are configurable output driving current.

There are up to 80 General Purpose I/O pins, GPIO, named from PA0~PA15 to PE0~PE15 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

2.11 Motor Control Timer - MCTM

- Two 16-bit up, down, up/down auto-reload counters
- 16-bit programmable prescaler allowing division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge aligned and center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Supports 3-phase motor control and hall sensor interface
- Brake input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter; four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM supports an Encoder interface controller to an incremental encoder with two inputs. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

2.12 PWM Generation and Capture Timers - GPTM

- One 16-bit up, down, up/down auto-reload counters
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and

several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

2.13 Basic Function Timer - BFTM

- Two 32-bit compare/match count-up counters - no I/O control features
- One shot mode - counting stops after a match condition
- Repetitive mode - restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

2.14 Watchdog Timer - WDT

- 12-bit down counter with 3-bit prescaler
- Interrupt or reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and a WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before a Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

2.15 Real Time Clock - RTC

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC for short, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD18} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD15} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wake-up timer to generate a system resume signal from the Power-Down mode.

2.16 Inter-integrated Circuit - I2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 1. 100 kHz in the Standard mode, 2. 400 kHz in the Fast mode and 3. 1 MHz in the Fast mode plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C module also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

2.17 Serial Peripheral Interface - SPI

- Supports both master and slave mode
- Frequency of up to ($f_{PCLK}/2$) MHz for master mode and ($f_{PCLK}/3$) MHz for slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

2.18 Universal Synchronous Asynchronous Receiver Transmitter - USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to $(f_{PCLK}/16)$ MHz and synchronous operating rate up to $(f_{PCLK}/8)$ MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode - RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 16 x 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a 16-byte transmitter FIFO, (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

2.19 Universal Asynchronous Receiver Transmitter - UART

- Asynchronous serial communication operating baud-rate up to ($f_{PCLK}/16$) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

2.20 Smart Card Interface - SCI

- Supports ISO 7816-3 standard
- Character mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface is compatible with the ISO 7816-3 standard. This interface includes Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform all the necessary Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

2.21 Inter-IC Sound – I2S

- Master or slave mode
- Mono and stereo
- I2S-justified, Left-justified, and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 x 32-bit Tx & Rx FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I2S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I2S supports a variety of data formats. In addition to the stereo I2S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I2S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

2.22 Cyclic Redundancy Check - CRC

- Support CRC16 polynomial: 0x8005,
 $X^{16}+X^{15}+X^2+1$
- Support CCITT CRC16 polynomial: 0x1021,
 $X^{16}+X^{12}+X^5+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
 $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored.

Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means data stream contains a data error.

2.23 Peripheral Direct Memory Access - PDMA

- 12 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:
ADC, SPI, EBI, CRC, USART, UART, I2C, I2S, GPTM, M2TM, SCI, AES, SDIO and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to join each data movement operation.

2.24 External Bus Interface - EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Memory bank regions and independent chip select control for each memory bank
- Programmable timings to support a wide range of devices
- Includes page read mode
- Automatic translation when the AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
 - Up to 25 address lines
 - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the internal address map of the CPU. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8 or 16-bit bus interface.

2.25 Universal Serial Bus Device Controller - USB

- Complies with USB 2.0 full-speed (12Mbps) specification

- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP-SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

2.26 CMOS Sensor Interface - CSIF (HT32F22366 only)

- Up to 2048 x 2048 input resolution
- Supports 8-bit YUV422 and Raw RGB formats
- Up to 24 MHz input pixel clock frequency
- Multi VSYNC and HSYNC settings for image capture
- Hardware window capture function
- Fractional hardware sub-sample function
- Dual FIFOs each with a capacity of 8 x 32 bits which can be read by the PDMA or CPU

The CMOS Sensor Interface, otherwise known as the CSIF, provides an interface for image capture from CMOS sensors. The device can be connected to the CMOS sensor directly using its CMOS Sensor Interface. The CSIF supports both Vertical SYNC and Horizontal SYNC modes for image capture implementation. The CSIF consists of window capture and sub-sampling functions together with dual FIFOs, each with a capacity of 8 x 32 bits, to store data which can be moved to the internal SRAM via the Peripheral Direct Memory Access circuitry, PDMA. The CSIF does not support image data conversion or decode but rather transfers the image data received from the CMOS sensor to the internal SRAM transparently.

2.27 Advanced Encryption Standard - AES

- Support AES Encrypt / Decrypt Function
- Support AES ECB/CBC/CTR mode
- Support Key Size 128, 192 and 256 bits
- Support 4 words Initial Vector for CBC and CTR mode
- 8 x 32bits (Each IN and OUT FIFO Capacity) for 2 AES Data blocks

- Support DMA Interface
- Support Word Data Swap Function

The AES core supports encryption and decryption function. AES only supports 128 bits input data to do encryption or decryption. Hardware does not pad any bits of input data. Software need to do pad action at first.

2.28 Secure Digital Input Output - SDIO

2.29 Debug Support

- Serial Wire or JTAG Debug Port SWJ-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patches
- 4 comparators for hardware watchpoints
- 1-bit asynchronous trace for serial wire debug mode – TRACESWO

2.30 Package and Operation Temperature

- 48/64/100-pin LQFP package
- Operation temperature range: -40°C to +85°C

3 Overview

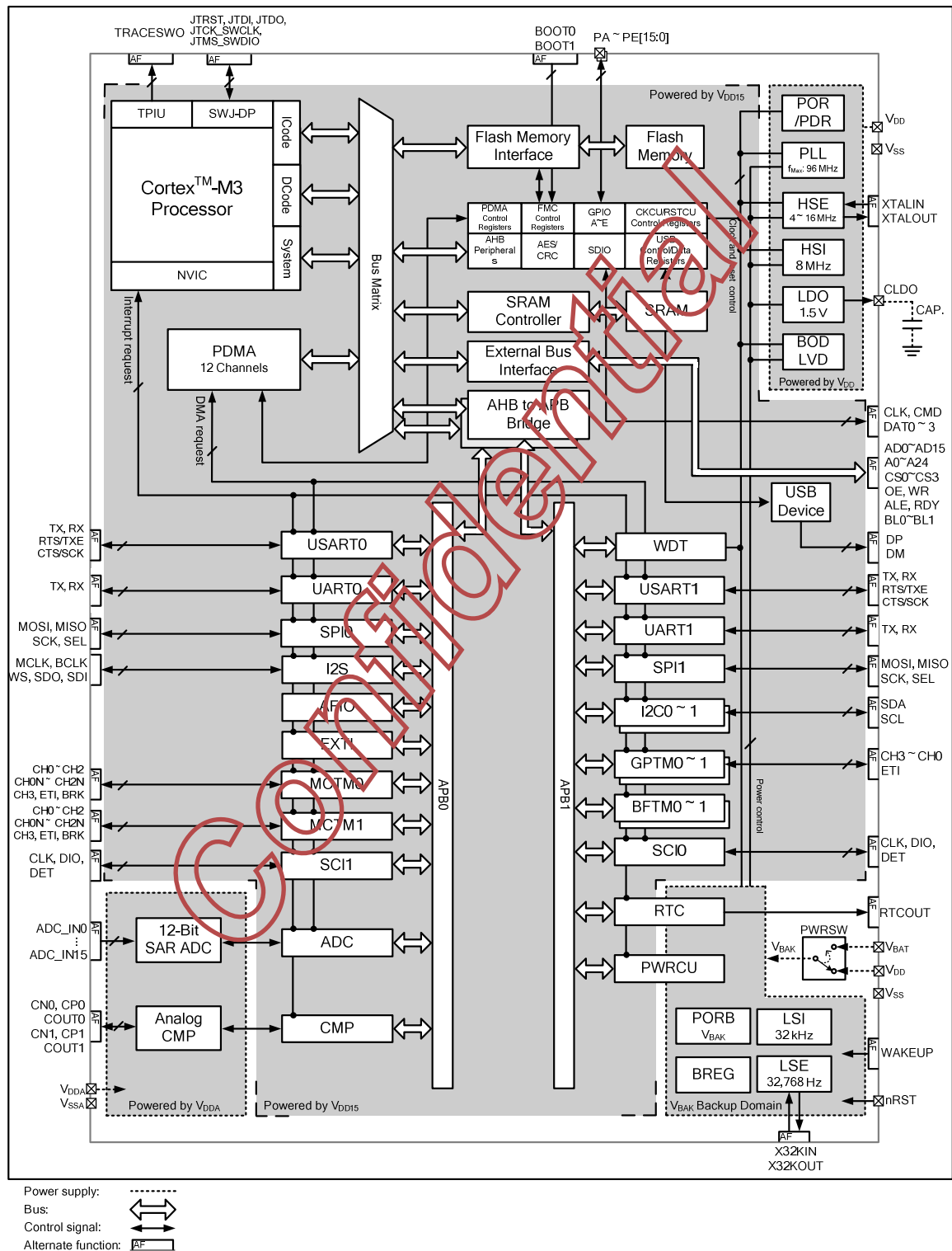
3.1 Device Information

Table 1 HT32F12365/12366/22366 Features and Peripheral List

Peripherals		HT32F12365	HT32F12366	HT32F22366
Main Flash (KB)		255	255	255
Option Bytes Flash (KB)		1	1	1
SRAM (KB)		64	128	128
Timers	MCTM		2	
	GPTM		2	
	BFTM		2	
	RTC		1	
	WDT		1	
Communication	CSIF			1
	USB		1	
	SCI		2	
	USART		2	
	UART		2	
	SPI		2	
	I ² C		2	
	I ² S		1	
PDMA			12 channels	
AES			1	
SDIO			1	
EBI			1	
CRC			1	
GPIO			Up to 80	
EXTI			16	
12-bit ADC			1	
Number of channels			Max. 16 Channels	
Comparator			2	
CPU frequency			Up to 96 MHz	
Operating voltage			2.0 V ~ 3.6 V	
Operating temperature			-40 °C ~ +85 °C	
Package			48/64/100-pin LQFP	

3.2 Block Diagram

Figure 1 HT32F12365/12366/22366 Block Diagram



3.3 Memory Map

Figure 2 HT32F12365/12366/22366 Memory Map

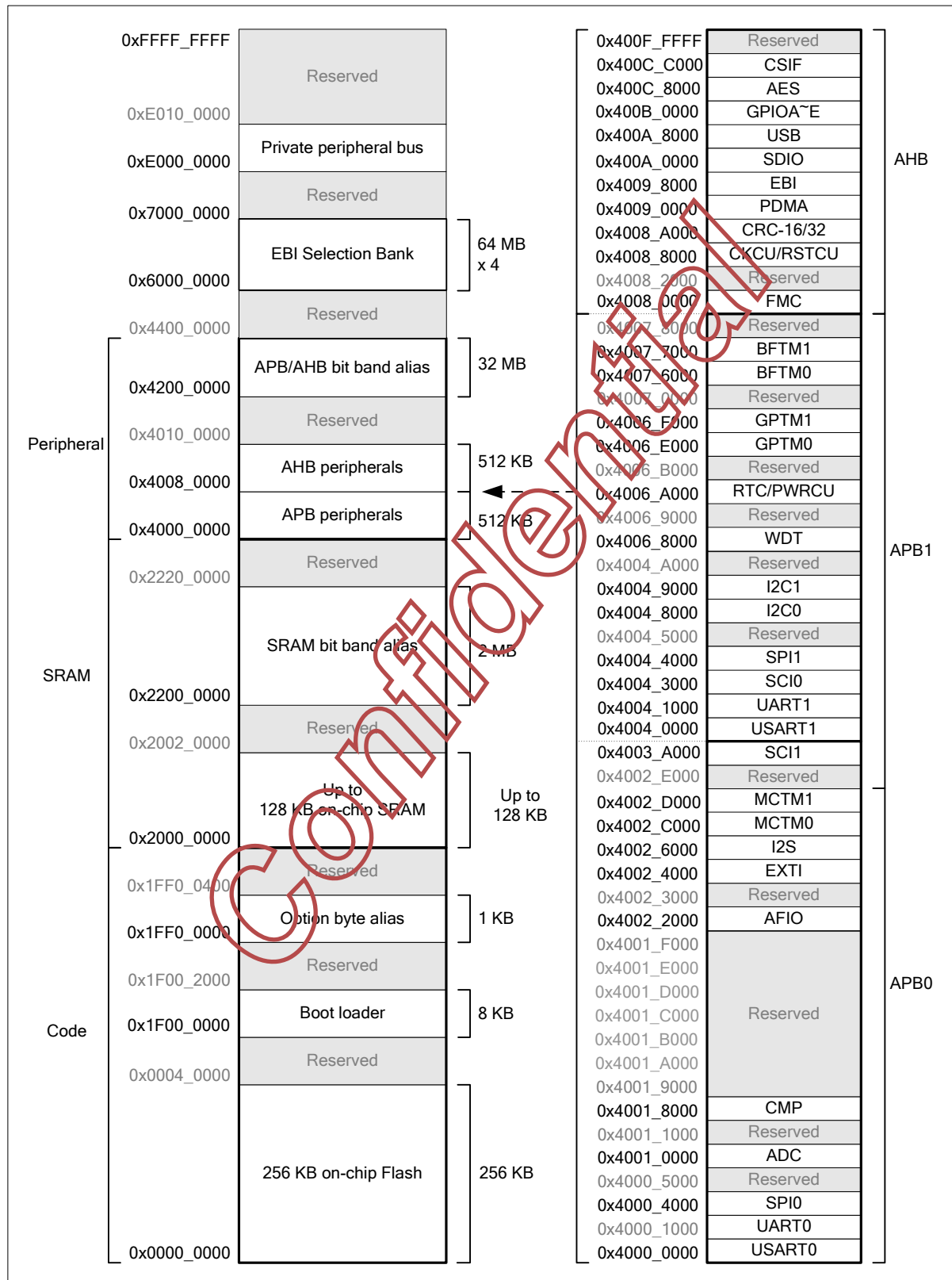


Table 2 HT32F12365/12366/22366 Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART0	APB0
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4001_9FFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_6000	0x4002_6FFF	I2S	
0x4002_7000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM0	
0x4002_D000	0x4002_DFFF	MCTM1	
0x4002_E000	0x4003_AFFF	Reserved	
0x4003_A000	0x4003_AFFF	SCI1	
0x4003_C000	0x4003_FFFF	Reserved	
0x4004_0000	0x4004_0FFF	USART1	APB1
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI0	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I2C0	
0x4004_9000	0x4004_9FFF	I2C1	
0x4004_A000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	Comparator	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM0	

Start Address	End Address	Peripheral	Bus
0x4006_F000	0x4006_FFFF	GPTM1	
0x4007_0000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA Control Registers	
0x4009_2000	0x400C_BFFF	Reserved	
0x4009_8000	0x4009_9FFF	EBI Control Registers	
0x4009_A000	0x4009_FFFF	Reserved	
0x400A_0000	0x400A_1FFF	SDIO	
0x400A_2000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_BFFF	USB	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400B_9FFF	GPIOE	
0x400B_A000	0x400C_7FFF	Reserved	
0x400C_8000	0x400C_9FFF	AES	
0x400C_A000	0x400C_BFFF	Reserved	
0x400C_C000	0x400C_DFFF	CSIF	
0x400C_E000	0x400F_FFFF	Reserved	

Figure 5 HT32F12365/12366/22366 LQFP-64 Pin Assignment

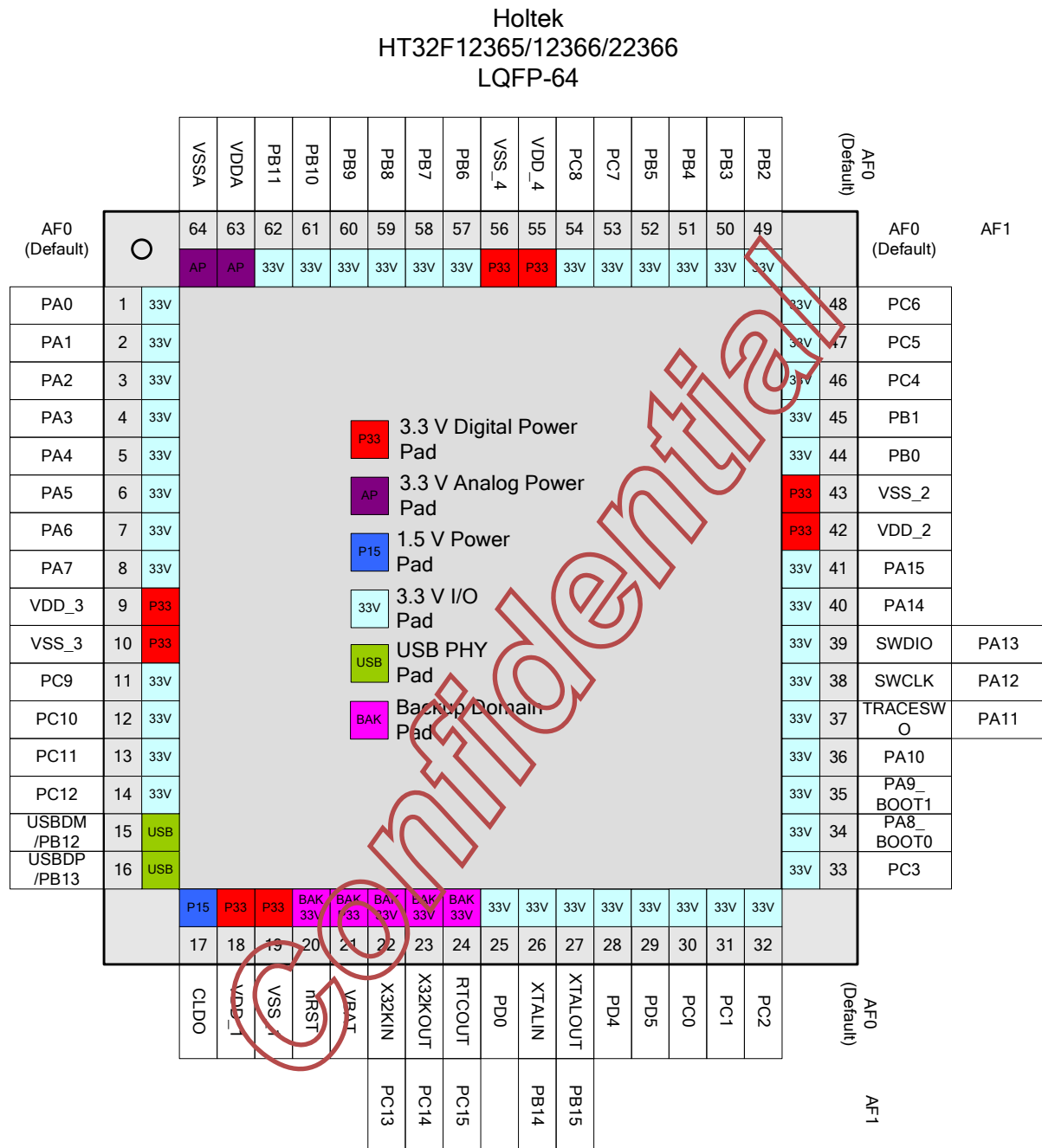


Figure 6 HT32F12365/12366/22366 LQFP-100 Pin Assignment

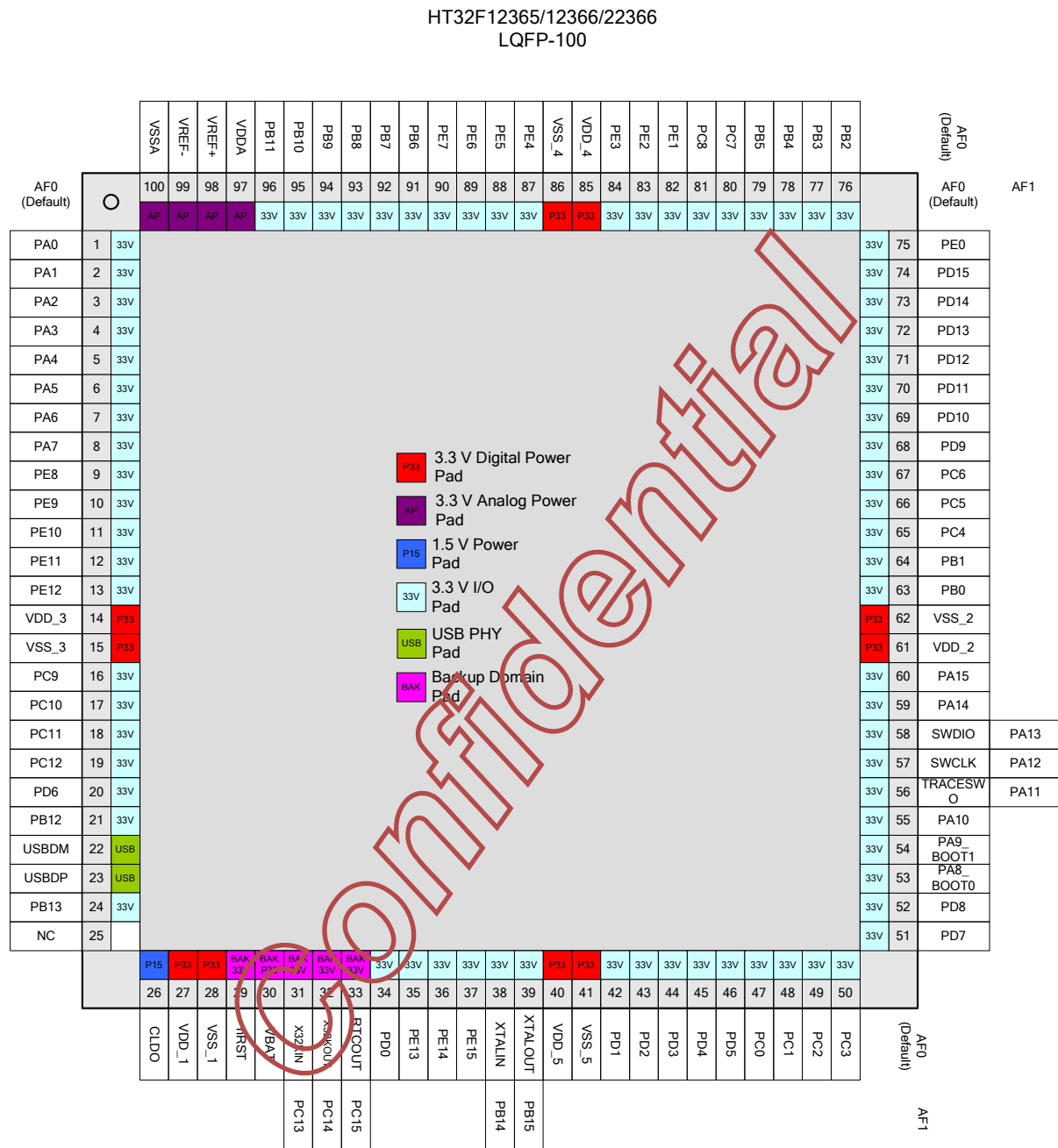


Table 3 HT32F12365/12366/22366 Series Pin Assignment for LQFP 64 / 48 Package

Package			Alternate function number															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
LQFP -100	LQFP -64	LQFP -48	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I2C	SCI	EBI	I2S	SDIO	CSIF	N/A	N/A	System Other
1	1	1	PA0		ADC_IN0		GT1_CH0	SPI1_SCK	USR0_RTS	I2C1_SCL	SCI0_CLK		I2S_WS		CSIF_D0			
2	2	2	PA1		ADC_IN1		GT1_CH1	SPI1_MOSI	USR0_CTS	I2C1_SDA	SCI0_DIO		I2S_BCLK	SD_DAT1	CSIF_D1			
3	3	3	PA2		ADC_IN2		GT1_CH2	SPI1_MISO	USR0_TX				I2S_SDO	SD_DAT2	CSIF_D2			
4	4	4	PA3		ADC_IN3		GT1_CH3	SPI1_SEL	USR0_RX				I2S_SDI	SD_DAT3	CSIF_D3			
5	5	5	PA4		ADC_IN4		GT0_CH0	SPI0_SCK	USR1_TX	I2C0_SCL	SCI1_CLK			SD_CMD	CSIF_D4			
6	6	6	PA5		ADC_IN5		GT0_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA	SCI1_DIO			SD_CLK	CSIF_D5			
7	7	7	PA6		ADC_IN6		GT0_CH2	SPI0_MISO	USR1_RTS		SCI1_DET			SD_DAT0	CSIF_D6			
8	8	8	PA7		ADC_IN7		GT0_CH3	SPI0_SEL	USR1_CTS				I2S_MCLK		CSIF_D7			
9			PE8		ADC_IN8			SPI1_SEL	USR0_RTS						CSIF_HSYN C			
10			PE9		ADC_IN9			SPI1_SCK	USR0_CTS						CSIF_VSYN C			
11			PE10		ADC_IN10			SPI1_MOSI	USR0_TX						CSIF_PCK			
12			PE11		ADC_IN11			SPI1_MISO	USR0_RX						CSIF_MCK			
13			PE12		ADC_IN12													
14	9	9	VDD_3															
15	10	10	VSS_3															
16	11		PC9		ADC_IN13		GT0_CH0	SPI1_SEL	UR0_TX	I2C1_SCL				SD_DAT0	CSIF_HSYN C			
17	12		PC10		ADC_IN14		GT0_CH1	SPI1_SCK	UR0_RX	I2C1_SDA				SD_DAT1	CSIF_VSYN C			
18	13		PC11		ADC_IN15		GT0_CH2	SPI1_MOSI						SD_DAT2	CSIF_PCK			
19	14		PC12				GT0_CH3	SPI1_MISO						SD_DAT3	CSIF_MCK			
20			PD6				GT0_ETI					EBI_NRDY						
21	15	11	PB12				MT1_CH2		USR0_TX	I2C0_SCL					CSIF_D7			
22	15	11	USBDM															
23	16	12	USBDP															
24	16	12	PB13				MT1_CH2N		USR0_RX	I2C0_SDA					CSIF_D6			
25			N.C.															

Package			Alternate function number															
LQFP -100	LQFP -64	LQFP -48	AF0 System Default	AF1 GPIO	AF2 ADC	AF3 CMP	AF4 MCTM /GPTM	AF5 SPI	AF6 USART /UART	AF7 I2C	AF8 SCI	AF9 EBI	AF10 I2S	AF11 SDIO	AF12 CSIF	AF13 N/A	AF14 N/A	AF15 System Other
26	17	13	CLDO															
27	18	14	VDD_1															
28	19	15	VSS_1															
29	20	16	nRST															
30	21	17	VBAT															
31	22	18	X32KIN	PC13														
32	23	19	X32K OUT	PC14														
33	24	20	RTCOUT	PC15														WAKEUP
34	25		PD0				MT1_ETI			I2C0_SDA		EBI_A18	I2S_SDI	SD_CMD				
35			PE13							I2C0_SCL		EBI_A19	I2S_MCLK					
36			PE14				GT1_ETI					EBI_A20	I2S_WS					
37			PE15				GT1_CH0		UR0_TX			EBI_A21						
38	26	21	XTALIN	PB14														
39	27	22	XTALOUT	PB15														
40			VDD_5															
41			VSS_5															
42			PD1				GT1_CH1		UR0_RX			EBI_A22	I2S_BCLK					
43			PD2				GT1_CH2					EBI_A23	I2S_SDO					
44			PD3				GT1_CH3					EBI_A24	I2S_SD					
45	28	23	PD4				MT1_CH0	SPIO_SEL		I2C1_SCL	SCI1_CLK	EBI_A16	I2S_MCLK	SD_CLK	CSIF_D5			
46	29	24	PD5				MT1_CH0N	SPIO_SCK		I2C1_SDA	SCI1_DIO	EBI_A17		SD_CMD	CSIF_D4			
47	30		PC0				GT1_CH0	SPI1_SEL				EBI_AD13	I2S_WS	SD_DAT1				
48	31		PC1				GT1_CH1	SPI1_SCK				EBI_AD14	I2S_BCLK	SD_DAT2				
49	32		PC2				GT1_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL		EBI_AD15	I2S_SDO	SD_DAT3				
50	33		PC3				GT1_CH3	SPI1_MISO	UR1_RX	I2C0_SDA	SCI1_DET	EBI_CS3	I2S_SDI	SD_DAT0				

Package			Alternate function number															
LQFP -100	LQFP -64	LQFP -48	AF0 System Default	AF1 GPIO	AF2 ADC	AF3 CMP	AF4 MCTM /GPTM	AF5 SPI	AF6 USART /UART	AF7 I2C	AF8 SCI	AF9 EBI	AF10 I2S	AF11 SDIO	AF12 CSIF	AF13 N/A	AF14 N/A	AF15 System Other
51			PD7							I2C1_SCL		EBI_A2						
52			PD8							I2C1_SDA		EBI_A0						
53	34	25	PA8_BOOT0						USR0_TX		SCI1_CLK		I2S_MCLK					CKOUT
54	35	26	PA9_BOOT1					SPI0_MOSI			SCI1_DIO	EBI_A1	I2S_WS					
55	36	27	PA10				MT1_CH1		USR0_RX		SCI0_DET			SD_DAT0	CSIF_D7			
56	37	28	JTDO	PA11			MT1_CH1N	SPI0_MISO			SCI1_DET	EBI_A0	I2S_MCLK					TRACESWO
57	38	29	JTCK /SWCLK	PA12														
58	39	30	JTMS /SWDIO	PA13														
59	40	31	JTDI	PA14			MT0_CH0	SPI1_SEL	USR1_TX		SCI0_CLK	EBI_AD0			CSIF_HSYN C			
60	41	32	JTRST	PA15			MT0_CH0N	SPI1_SCK	USR1_RX		SCI0_DIO	EBI_AD1			CSIF_VSYNC			
61	42		VDD_2															
62	43		VSS_2															
63	44	33	PB0				MT0_CH1	SPI1_MOSI	USR0_TX	I2C0_SCL		EBI_AD2			CSIF_PCK			
64	45	34	PB1				MT0_CH1N	SPI1_MISO	USR0_RX	I2C0_SDA		EBI_AD3			CSIF_MCK			
65	46		PC4				MT1_CH2		USR1_RTS		SCI0_CLK	EBI_AD0		SD_CLK				
66	47		PC5				MT1_CH2N		USR1_CTS		SCI0_DIO	EBI_AD11		SD_CMD				
67	48		PC6				MT1_CH3				SCI0_DET	EBI_AD12		SD_DAT0				
68			PD9					SPI0_SEL				EBI_A3						
69			PD10					SPI0_SCK				EBI_A4						
70			PD11					SPI0_MOSI				EBI_A5						
71			PD12					SPI0_MISO				EBI_A6						
72			PD13					SPI1_SEL				EBI_A7						
73			PD14					SPI1_SCK				EBI_A8						
74			PD15					SPI1_MOSI				EBI_A9						
75			PE0					SPI1_MISO				EBI_A10						

Package			Alternate function number															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
LQFP -100	LQFP -64	LQFP -48	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I2C	SCI	EBI	I2S	SDIO	CSIF	N/A	N/A	System Other
		35	VDD_2															
		36	VSS_2															
76	49	37	PB2				MT0_CH2	SPI0_SEL	UR0_TX			EBI_AD4			CSIF_D0			
77	50	38	PB3				MT0_CH2N	SPI0_SCK	UR0_RX			EBI_AD5			CSIF_D1			
78	51	39	PB4				MT0_BRK	SPI0_MOSI	UR1_TX			EBI_AD6			CSIF_D2			
79	52	40	PB5				MT1_BRK	SPI0_MISO	UR1_RX			EBI_AD7			CSIF_D3			
80	53		PC7				MT0_CH3			I2C0_SCL		EBI_AD8		SD_CMD				
81	54		PC8				MT0_F1			I2C0_SDA		EBI_AD9		SD_CLK				
82			PE1				MT1_CH0		USR1_TX		SCI0_CLK	EBI_A11						
83			PE2				MT1_CH0N				SCI0_DIO	EBI_A12						
84			PE3				MT1_CH1					EBI_A13						
85	55		VDD_4															
86	56		VSS_4															
87			PE4				MT1_CH1N			I2C1_SCL		EBI_A14		SD_DAT0				
88			PE5				MT1_CH2		USR1_RX	I2C1_SDA		EBI_A15		SD_DAT1				
89			PE6				MT1_CH2N		USR1_RTS			EBI_B10	I2S_BCLK	SD_DAT2				
90			PE7				MT1_BRK		USR1_CTS			EBI_B11	I2S_MCLK	SD_DAT3				
91	57	41	PB6			CN0	MT1_CH0	SPI1_SEL	UR1_TX			EBI_QE	I2S_MCLK		CSIF_D4			
92	58	42	PB7			CP0	MT1_CH0N	SPI1_SCK				EBI_CS0			CSIF_D5			
93	59	43	PB8			COUT0		SPI1_MOSI	UR1_RX			EBI_WE			CSIF_D6			
94	60	44	PB9			CN1	MT1_CH2	SPI1_MISO	UR0_TX		SCI1_CLK	EBI_ALE	I2S_BCLK	SD_DAT1	CSIF_D7			
95	61	45	PB10			CP1	MT1_CH2N			I2C1_SCL	SCI1_DET	EBI_CS1	I2S_SDO	SD_DAT2				
96	62	46	PB11			COUT1	MT1_CH3		UR0_RX	I2C1_SDA	SCI1_DIO	EBI_CS2	I2S_SDI	SD_DAT3				
97	63	47	VDDA															
98			VREF+															
99			VREF-															
100	64	48	VSSA															

Table 4 HT32F12365/12366/22366 Pin Description

			Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
LQFP 100	LQFP 64	LQFP 48					Default function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9			PE8	AI/O	33V	4/8/12/16 mA	PE8
10			PE9	AI/O	33V	4/8/12/16 mA	PE9
11			PE10	AI/O	33V	4/8/12/16 mA	PE10
12			PE11	AI/O	33V	4/8/12/16 mA	PE11
13			PE12	AI/O	33V	4/8/12/16 mA	PE12
14	9	9	VDD_3	P	--	--	Voltage for digital I/O
15	10	10	VSS_3	P	--	--	Ground reference for digital I/O
16	11		PC9	AI/O	33V	4/8/12/16 mA	PC9
17	12		PC10	AI/O	33V	4/8/12/16 mA	PC10
18	13		PC11	AI/O	33V	4/8/12/16 mA	PC11
19	14		PC12	AI/O	33V	4/8/12/16 mA	PC12
20			PD6	AI/O	33V	4/8/12/16 mA	PD6
21	15	11	PB12	I/O	33V	4/8/12/16 mA	PB12
22	15	11	USBDM	AI/O	--	--	USB Differential data bus conforming to the Universal Serial Bus standard.
23	16	12	USBDP	AI/O	--	--	USB Differential data bus conforming to the Universal Serial Bus standard.
24	16	12	PB13	I/O	33V	4/8/12/16 mA	PC7
25			N.C.				N.C.
26	17	13	CLDO	P	--	--	Core power LDO 1.5 V output. It is recommended to connect a 1 uF capacitor as close as possible between this pin and VSS_1.
27	18	14	VDD_1	P	--	--	Voltage for digital I/O
28	19	15	VSS_1	P	--	--	Ground reference for digital I/O
29	20	16	nRST	I (BK)	33V_PU	--	External reset pin and external wakeup pin in the Power-Down mode
30	21	17	VBAT	P	--	--	Battery power input for the backup domain
31	22	18	PC13 ^{Note 4}	AI/O (BK)	33V	< 2 mA	X32KIN
32	23	19	PC14 ^{Note 4}	AI/O (BK)	33V	< 2 mA	X32KOUT
33	24	20	PC15 ^{Note 4}	I/O (BK)	33V	< 2 mA	RTCOUT
34	25		PD0	I/O	33V	4/8/12/16 mA	PD0
35			PE13	I/O	33V	4/8/12/16 mA	PE13
36			PE14	I/O	33V	4/8/12/16 mA	PE14
37			PE15	I/O	33V	4/8/12/16 mA	PE15
38	26	21	PB14	AI/O	33V	4/8/12/16 mA	XTALIN
39	27	22	PB15	AI/O	33V	4/8/12/16 mA	XTALOUT
40			VDD_5	P	--	--	Voltage for digital I/O
41			VSS_5	P	--	--	Ground reference for digital I/O
42			PD1	I/O	33V	4/8/12/16 mA	PD1
43			PD2	I/O	33V	4/8/12/16 mA	PD2
44			PD3	I/O	33V	4/8/12/16 mA	PD3
45	28	23	PD4	I/O	33V	4/8/12/16 mA	PD4
46	29	24	PD5	I/O	33V	4/8/12/16 mA	PD5
47	30		PC0	I/O	33V	4/8/12/16 mA	PC0
48	31		PC1	I/O	33V	4/8/12/16 mA	PC1
49	32		PC2	I/O	33V	4/8/12/16 mA	PC2

LQFP 100	LQFP 64	LQFP 48	Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
							Default function (AF0)
50	33		PC3	I/O	33V	4/8/12/16 mA	PC3
51			PD7	I/O	33V	4/8/12/16 mA	PD7
52			PD8	I/O	33V	4/8/12/16 mA	PD8
53	34	25	PA8	I/O	33V_PU	4/8/12/16 mA	PA8_BOOT0
54	35	26	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT1
55	36	27	PA10	I/O	33V	4/8/12/16 mA	PA10
56	37	28	PA11	I/O	33V	4/8/12/16 mA	JTDO/TRACESWO
57	38	29	PA12	I/O	33V_PU	4/8/12/16 mA	JTCK/SWCLK
58	39	30	PA13	I/O	33V_PU	4/8/12/16 mA	JTMS/SWDIO
59	40	31	PA14	I/O	33V_PU	4/8/12/16 mA	JTDI
60	41	32	PA15	I/O	33V_PU	4/8/12/16 mA	JTRST
61	42		VDD_2	P	--	--	Voltage for digital I/O
62	43		VSS_2	P	--	--	Ground reference for digital I/O
63	44	33	PB0	I/O	33V	4/8/12/16 mA	PB0
64	45	34	PB1	I/O	33V	4/8/12/16 mA	PB1
65	46		PC4	I/O	33V	4/8/12/16 mA	PC4
66	47		PC5	I/O	33V	4/8/12/16 mA	PC5
67	48		PC6	I/O	33V	4/8/12/16 mA	PC6
68			PD9	I/O	33V	4/8/12/16 mA	PD9
69			PD10	I/O	33V	4/8/12/16 mA	PD10
70			PD11	I/O	33V	4/8/12/16 mA	PD11
71			PD12	I/O	33V	4/8/12/16 mA	PD12
72			PD13	I/O	33V	4/8/12/16 mA	PD13
73			PD14	I/O	33V	4/8/12/16 mA	PD14
74			PD15	I/O	33V	4/8/12/16 mA	PD15
75			PE0	I/O	33V	4/8/12/16 mA	PE0
		35	VDD_2	P	--	--	Voltage for digital I/O
		36	VSS_2	P	--	--	Ground reference for digital I/O
76	49	37	PB2	I/O	33V	4/8/12/16 mA	PB2
77	50	38	PB3	I/O	33V	4/8/12/16 mA	PB3
78	51	39	PB4	I/O	33V	4/8/12/16 mA	PB4
79	52	40	PB5	I/O	33V	4/8/12/16 mA	PB5
80	53		PC7	I/O	33V	4/8/12/16 mA	PC7
81	54		PC8	I/O	33V	4/8/12/16 mA	PC8
82			PE1	I/O	33V	4/8/12/16 mA	PE1
83			PE2	I/O	33V	4/8/12/16 mA	PE2
84			PE3	I/O	33V	4/8/12/16 mA	PE3
85	55		VDD_4	P	--	--	Voltage for digital I/O
86	56		VSS_4	P	--	--	Ground reference for digital I/O
87			PE4	I/O	33V	4/8/12/16 mA	PE4
88			PE5	I/O	33V	4/8/12/16 mA	PE5
89			PE6	I/O	33V	4/8/12/16 mA	PE6
90			PE7	I/O	33V	4/8/12/16 mA	PE7
91	57	41	PB6	AI/O	33V	4/8/12/16 mA	PB6
92	58	42	PB7	AI/O	33V	4/8/12/16 mA	PB7
93	59	43	PB8	AI/O	33V	4/8/12/16 mA	PB8
94	60	44	PB9	AI/O	33V	4/8/12/16 mA	PB9
95	61	45	PB10	AI/O	33V	4/8/12/16 mA	PB10
96	62	46	PB11	AI/O	33V	4/8/12/16 mA	PB11
97	63	47	VDDA	P	--	--	Analog voltage for ADC and Comparator
98			VREF+	P	--	--	ADC positive reference voltage has to be lower or equal to VDDA
99			VREF-	P	--	--	ADC negative reference voltage has to be directly connected to VSSA
100	64	48	VSSA	P	--	--	Ground reference for the ADC and Comparator

Note:

1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, BK = Back-up domain
2. 33V = 3.3 V tolerant.
3. The GPIOs are in an AF0 state after a V_{DD15} power on reset (POR) except for the RTCOUT pin in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by the Backup Domain software reset (BAK_RST bit in BAK_CR register).

4. The backup domain of the I/O pins have a source current capability limitation of $< 2 \text{ mA}$ @ $V_{DD} = 3.3 \text{ V}$ and sink current typical is $4/8 \text{ mA}$ configurable @ $V_{DD} = 3.3 \text{ V}$.

Confidential

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{DD}	External main supply voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{DDA}	External analog supply voltage	V _{SSA} - 0.3	V _{SSA} + 3.6	V
V _{BAT}	External battery supply voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{IN}	Input voltage on 5 V-tolerant I/O	V _{SS} - 0.3	V _{SS} + 5.5	V
V _{IN}	Input voltage on other I/O	V _{SS} - 0.3	V _{DD} + 0.3	V
TA	Ambient operating temperature range	-40	+85	°C
TSTG	Storage temperature range	-55	+150	°C
TJ	Maximum junction temperature		125	°C
PD	Total power dissipation		500	mW
VESD	Electrostatic discharge voltage - human body mode	-4000	+4000	V

5.2 Recommended DC Operating Conditions

Table 6 Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	I/O operating voltage		2.0	3.3	3.6	V
V _{DDA}	Analog operating voltage		2.5	3.3	3.6	V
V _{BAT}	Battery supply operating voltage		2.0	3.3	3.6	V

5.3 On-Chip LDO Voltage Regulator Characteristics

Table 7 LDO Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDO}	Internal regulator output voltage	$V_{DD} \geq 2.0\text{ V}$ Regulator input @ $I_{LDO} = 35\text{ mA}$ and voltage variant = $\pm 5\%$, After trimming.	1.425	1.5	1.57	V
I_{LDO}	Output current	$V_{DD} = 2.0\text{ V}$ Regulator input @ $V_{LDO} = 1.5\text{ V}$	-	75	--	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent on the core power current consumption	-	2.2	-	μF

5.4 Power Consumption

Table 8 Power Consumption Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	$V_{DD} = V_{BAT} = 3.3\text{ V}$, HSE = 8 MHz, PLL = 48 MHz, $f_{HCLK} = 48\text{ MHz}$, $f_{PCLK} = 48\text{ MHz}$, All peripherals enabled	-		-	mA
		$V_{DD} = V_{BAT} = 3.3\text{ V}$, HSE = 8 MHz, PLL = 48 MHz, $f_{HCLK} = 48\text{ MHz}$, $f_{PCLK} = 48\text{ MHz}$, All peripherals disabled	-		-	mA
	Supply current (Sleep mode)	$V_{DD} = V_{BAT} = 3.3\text{ V}$, HSE = 8 MHz, PLL = 48 MHz, $f_{HCLK} = 0\text{ MHz}$, $f_{PCLK} = 48\text{ MHz}$, All peripherals enabled	-		-	mA
		$V_{DD} = V_{BAT} = 3.3\text{ V}$, HSE = 8 MHz, PLL = 48 MHz, $f_{HCLK} = 0\text{ MHz}$, $f_{PCLK} = 48\text{ MHz}$, All peripherals disabled	-		-	mA
	Supply current (Deep-Sleep1 mode)	$V_{DD} = V_{BAT} = 3.3\text{ V}$, All clock off (HSE/PLL/ f_{HCLK}), LDO in low power mode, LSI on, RTC on	-		-	μA
	Supply current (Deep-Sleep2 mode)	$V_{DD} = V_{BAT} = 3.3\text{ V}$, All clock off (HSE/PLL/ f_{HCLK}), LDO off (DMOS on), LSI on, RTC on	-		-	μA
	Supply current (Power-Down mode)	$V_{DD} = V_{BAT} = 3.3\text{ V}$, LDO off, LSE on, LSI on, RTC on	-		-	μA
I_{BAT}	Battery supply current (Power-Down mode)	V_{DD33} not present, $V_{BAT} = 3.3\text{ V}$, LDO off, LSE off, LSI on, RTC on	-		-	μA
		V_{DD} not present, $V_{BAT} = 3.3\text{ V}$, LDO off, LSE off, LSI on, RTC off	-		-	μA

Note:

1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 KHz low speed external oscillator. LSI means 32 KHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

5.5 Reset and Supply Monitor Characteristics

Table 9 V_{DD} Power Reset Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold (Rising Voltage on V_{DD})	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	1.66	1.79	1.90	V
V_{PDR}	Power down reset threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
V_{PORHYS}	POR hysteresis			150		mV
T_{POR}	Reset delay time	$V_{DD} = 3.3\text{ V}$		0.1	0.2	ms

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO will be turn on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turn off.

Table 10 LVD/BOD Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{BOD}	Voltage of Brown Out Detection	T _A = -40 °C~ 85 °C After factory-trimmed (V _{DD} Falling edge)	2.02	2.1	2.18	V	
V _{LVD}	Voltage of Low Voltage Detection	T _A = -40 °C~ 85 °C (V _{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
V _{LVDHST}	LVD hysteresis	V _{DD} = 3.3 V		100		mV	
T _{suLVD}	LVD Setup time	V _{DD} = 3.3 V			5	us	
T _{atLVD}	LVD active delay time	V _{DD} = 3.3 V		--		us	
I _{DDLVD}	Operation current NOTE3	V _{DD} = 3.3 V		5	15	uA	

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in PWRCU LVDCSR register

5.6 External Clock Characteristics

Table 11 High Speed External Clock (HSE) Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range		2.0		3.6	V
f_{HSE}	High Speed External oscillator frequency (HSE)		4	-	16	MHz
C_{LHSE}	Load capacitance	$V_{DD} = 3.3\text{ V}$, $R_{ESR} = 100\text{ }\Omega$ @ 16 MHz	-	-	22	pF
R_{FHSE}	Internal feedback resistor between XTALIN and XTALOUT pins		-	1	-	M Ω
R_{ESR}	Equivalent Series Resistance*	$V_{DD} = 3.3\text{ V}$, $C_L = 12\text{ pF}$ @ 16 MHz, HSEDR = 0 $V_{DD} = 2.4\text{ V}$, $C_L = 12\text{ pF}$ @ 16 MHz, HSEDR = 1			160	Ω
D_{HSE}	HSE oscillator Duty cycle		40	-	60	%
I_{DDHSE}	HSE oscillator current consumption	$V_{DD} = 3.3\text{ V}$ @ 16 MHz	-	TBD	-	mA
I_{PDHSE}	HSE oscillator power down current	$V_{DD} = 3.3\text{ V}$	-	-	0.01	μA
t_{SUHSE}	HSE oscillator startup time	$V_{DD} = 3.3\text{ V}$	-	-	4	ms

Table 12 Low Speed External Clock (LSE) Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAK}	Operation Range		2.0		3.6	V
f_{CK_LSE}	Frequency of LSE	$V_{BAK} = 2.0\text{ V} \sim 3.6\text{ V}$	--	32.768	--	KHz
R_F	Internal feedback resistor			10		MΩ
R_{ESR}	Equivalent Series Resistance	$V_{BAK} = 3.3\text{ V}$	30		TBD	KΩ
C_L	Recommended load capacitances	$V_{BAK} = 3.3\text{ V}$	6		TBD	pF
I_{DDLSE}	Oscillator supply current (High current mode)	$f_{CK_LSE} = 32.768\text{ KHz}$, $R_{ESR} = 50\text{ K}\Omega$, $C_L \geq 7\text{ pF}$ $V_{BAK} = 2.0\text{ V} \sim 2.7\text{ V}$ $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$		3.3	6.3	μA
	Oscillator supply current (Low current mode)	$f_{CK_LSE} = 32.768\text{ KHz}$, $R_{ESR} = 50\text{ K}\Omega$, $C_L < 7\text{ pF}$ $V_{BAK} = 2.0\text{ V} \sim 3.6\text{ V}$ $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$		1.8	3.3	μA
	Power down current				0.01	μA
t_{SULSE}	Startup time (Low current mode)	$f_{CK_LSE} = 32.768\text{ KHz}$, $V_{BAK} = 2.7\text{ V} \sim 3.6\text{ V}$	--	2.5	--	s

Note : The following guidelines are recommended to increase the robustness of the crystal circuit of the HSE / LSE clock in the PCB layout phase :

1. The crystal oscillator should be located as close as possible to the MCU so that the trace length would be as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the frequently switching signal lines away from the crystal area to prevent the crosstalk.

5.7 Internal Clock Characteristics

Table 13 High Speed Internal Clock (HSI) Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range		2.0		3.6	V
f_{HSI}	Frequency of HSI	$V_{DD} = 3.3\text{ V}$ @ $25\text{ }^{\circ}\text{C}$	--	8	--	MHz
ACC_{HSI}	Frequency accuracy of the factory-calibrated HSI oscillator	$V_{DD} = 3.3\text{ V}$ $T_A = 25\text{ }^{\circ}\text{C}$	-2	--	2	%
		$V_{DD} = 2.5\text{ V} \sim 3.6\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	-3	--	3	%
		$V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$ $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	-4	--	4	%
Duty	Duty cycle	$f_{HSI} = 8\text{ MHz}$	35	--	65	%
I_{DDHSI}	Oscillator supply current	$f_{HSI} = 8\text{ MHz}$		300	500	μA
	Power down current				0.05	μA
t_{SUHSI}	Startup time	$f_{HSI} = 8\text{ MHz}$	-	-	10	μs

Table 14 Low Speed Internal Clock (LSI) Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	$V_{DD} = 3.3\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	21	32	43	kHz
ACC_{LSI}	Frequency accuracy of LSI	After factory-trimmed, $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$	-10	-	+10	%
$I_{DDL SI}$	LSI Oscillator Operating current	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$	-	0.4	0.8	μA
$t_{SUL SI}$	LSI Oscillator startup time	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$	-	-	100	μs

5.8 PLL Characteristics

Table 15 PLL Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{PLL IN}$	PLL input clock		4	-	16	MHz
f_{CK_PLL}	PLL output clock		64	-	96	MHz
t_{LOCK}	PLL lock time		-	200	-	μs

5.9 Memory Characteristics

Table 16 Flash Memory Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program/erase cycles before failure. (Endurance)	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	100	--	-	K cycles
T_{RET}	Data retention time	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	10	-	-	Years
t_{PROG}	Word programming time	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	20	-	-	μs
t_{ERASE}	Page erase time	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	2	-	-	ms
t_{MERASE}	Mass erase time	$T_A = -40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$	10	-	-	ms

5.10 I/O Port Characteristics

Table 17 I/O Port Characteristics

 $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	Low level input current	3.3 V IO	-	-	3	μA
		Reset pin	-	-	3	μA
I_{IH}	High level input current	3.3 V IO	-	-	3	μA
		Reset pin	-	-	3	μA
V_{IL}	Low level input voltage	3.3 V IO	- 0.5	-	$V_{DD}^* - 0.35$	V
		Reset pin	- 0.5	-	$V_{DD}^* - 0.35$	V
V_{IH}	High level input voltage	3.3 V IO	$V_{DD}^* - 0.65$	-	$V_{DD}^* + 0.5$	V
		Reset pin	$V_{DD}^* - 0.65$	-	$V_{DD}^* + 0.5$	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HYS}	Schmitt trigger input voltage hysteresis	3.3 V IO		0.12 * V_{DD}		mV
		Reset pin		0.12 * V_{DD}		mV
I_{OL}	Low level output current (GPIO Sink current)	3.3 V IO 4 mA drive, $V_{OL} = 0.4$ V	4	-	-	mA
		3.3 V IO 8 mA drive, $V_{OL} = 0.4$ V	8	-	-	mA
		3.3 V IO 12 mA drive, $V_{OL} = 0.4$ V	12	-	-	mA
		3.3 V IO 16 mA drive, $V_{OL} = 0.4$ V	16	-	-	mA
		Backup Domain IO drive @ $V_{DD} = 3.3$ V, $V_{OL} = 0.4$ V, PB10, PB11, PB12	4			mA
I_{OH}	High level output current (GPIO Source current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD} - 0.4$ V	4	-	-	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD} - 0.4$ V	8	-	-	mA
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD} - 0.4$ V	12	-	-	mA
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD} - 0.4$ V	16	-	-	mA
		Backup Domain IO drive @ $V_{DD} = 3.3$ V, $V_{OL} = V_{DD} - 0.4$ V, PB10, PB11, PB12.			2	mA
V_{OL}	Low level output voltage	3.3 V 4 mA drive IO, $I_{OL} = 4$ mA	-	-	0.4	V
		3.3 V 8 mA drive IO, $I_{OL} = 8$ mA	-	-	0.4	V
		3.3 V 12 mA drive IO, $I_{OL} = 12$ mA	-	-	0.4	V
		3.3 V 16 mA drive IO, $I_{OL} = 16$ mA	-	-	0.4	V
		Backup Domain IO Sink Current = 4 mA (Low driving strength)	$V_{DD} = 2.7$ V~ 3.6 V		0.4	V
			$V_{DD} = 2.0$ V~ 2.7 V		0.6	V
		Backup Domain IO Sink Current = 8 mA (High driving strength)	$V_{DD} = 2.7$ V~ 3.6 V		0.4	V
V_{OH}	High level output voltage		$V_{DD} = 2.0$ V~ 2.7 V		0.6	V
		3.3 V 4 mA drive IO, $I_{OH} = 4$ mA	$V_{DD} - 0.4$	-	-	V
		3.3 V 8 mA drive IO, $I_{OH} = 8$ mA	$V_{DD} - 0.4$	-	-	V
		3.3 V 12 mA drive IO, $I_{OH} = 12$ mA	$V_{DD} - 0.4$	-	-	V
		3.3 V 16 mA drive IO, $I_{OH} = 16$ mA	$V_{DD} - 0.4$	-	-	V
		Backup Domain IO Source Current = 2mA	$V_{DD} = 2.7$ V~ 3.6 V	2.4		V
R_{PU}	Internal pull-up resistor	3.3 V I/O		46		k Ω
		3.3 V I/O		46		k Ω

5.11 ADC Characteristics

Table 18 ADC Characteristics

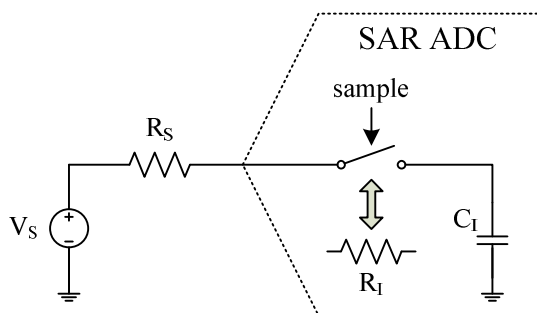
$T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.7	3.3	3.6	V
$V_{ADCI\text{N}}$	A/D Converter input voltage range		0	-	V_{REF+}	V
V_{REF+}	A/D Converter Reference voltage			V_{DDA}	V_{DDA}	V
I_{ADC}	Current consumption	$V_{DDA} = 3.3\text{ V}$	-	1	TBD	mA
I_{ADC_DN}	Power down current consumption	$V_{DDA} = 3.3\text{ V}$	-	-	0.1	μA
f_{ADC}	A/D Converter clock		0.7	-	16	MHz
f_S	Sampling rate		0.05	-	1	MHz
T_{DL}	Data latency			12.5		$1/f_{ADC}$ Cycles
$T_{S\&H}$	Sampling & hold time			3.5		$1/f_{ADC}$ Cycles
$T_{ADCCONV}$	A/D Converter conversion time		-	16	-	$1/f_{ADC}$ Cycles
R_I	Input sampling switch resistance		-	-	1	k Ω
C_I	Input sampling capacitance	No pin/pad capacitance included	-	16	-	pF
t_{SU}	Startup up time		-	-	1	μs
N	Resolution		-	12	-	bits
INL	Integral Non-linearity error	$f_S = 750\text{ KHz}$, $V_{DDA} = 3.3\text{ V}$	-	± 2	± 5	LSB
DNL	Differential Non-linearity error	$f_S = 750\text{ KHz}$, $V_{DDA} = 3.3\text{ V}$	-	± 1		LSB
E_O	Offset error		-	-	± 10	LSB
E_G	Gain error		-	-	± 10	LSB

Note:

1. Guaranteed by design, not tested in production.
2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S . Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I , must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S may not have an arbitrarily large value.

Figure 7 ADC Sampling Network Model



The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below $\frac{1}{4}$ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

5.12 Comparator Characteristics

Table 19 Comparator Characteristics

$T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	Comparator mode	2.4	3.3	3.6	V
V_{IN}	Input Common Mode Voltage Range	CP or CN	V_{SSA}		V_{DDA}	V
V_{IOS}	Input offset voltage ⁽¹⁾	$T_A = 25^\circ\text{C}$	-15	-	15	mV
V_{hys}	Input Hysteresis	No hysteresis (CMPnHM [1:0] = 00)		0		mV
		Low hysteresis (CMPnHM [1:0] = 01)		30		mV
		Middle hysteresis (CMPnHM [1:0] = 10)		70		mV
		High hysteresis (CMPnHM [1:0] = 11)		100		mV
t_{RT}	Response time Input Overdrive = $\pm 100\text{mV}$	High Speed mode $V_{DDA} \geq 2.7\text{V}$		50	100	ns
		$V_{DDA} < 2.7\text{V}$		100	250	
		Low Speed mode		2	5	us
I_{CMP}	Current Consumption $V_{DDA} = 3.3\text{V}$	High Speed mode		130		uA
		Low Speed mode		30		uA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid.			50	us
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0 CVREFEN = 0 CVREFOE=0			0.1	uA
Comparator Voltage Reference (CVR)						
V_{CVR}	Output Range		V_{SSA}		V_{DDA}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N _{Bits}	CVR Scaler Resolution			6		bits
t _{CVRST}	Setting Time	CVR scaler setting time from CVREF = "000000" to "111111"			100	us
I _{CVR}	Current Consumption V _{DDA} = 3.3 V	CVREFEN=1, CMPREFOE=0		65		uA
		CVREFEN=1, CVREFOE=1		80	110	uA

1. Guaranteed by design, not tested in production.

5.13 GPTM/MCTM Characteristics

Table 20 SCTM/GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{TM}	Timer clock source for GPTM and MCTM	-	-	-	48	MHz
t _{RES}	Timer resolution time	-	-	-	-	f _{TM}
f _{EXT}	External single frequency on channel 1 ~ 4	-	-	-	1/2	f _{TM}
RES	Timer resolution	-	-	-	16	bits

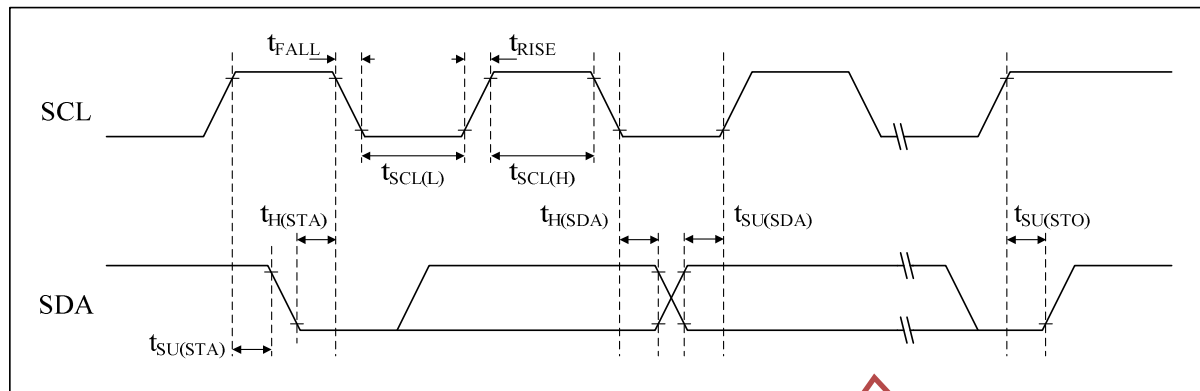
5.14 I²C Characteristics

Table 21 I²C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
f _{SCL}	SCL clock frequency	-	100	-	400	-	1000	kHz
t _{SCL(H)}	SCL clock high time	4.5		1.125		0.45		μs
t _{SCL(L)}	SCL clock low time	4.5		1.125		0.45		μs
t _{FALL}	SCL and SDA fall time		1.3		0.34		0.135	μs
t _{RISE}	SCL and SDA rise time		1.3		0.34		0.135	μs
t _{SU(SDA)}	SDA data setup time	500		125		50		ns
t _{H(SDA)}	SDA data hold time	0		0		0		ns
t _{SU(STA)}	START condition setup time	500		125		50		ns
t _{H(STA)}	START condition hold time	0		0		0		ns
t _{SU(STO)}	STOP condition setup time	500		125		50		ns

- Guaranteed by design, not tested in production.
- To achieve 100kHz standard mode, the peripheral clock frequency must be higher than 2MHz.
- To achieve 400kHz fast mode, the peripheral clock frequency must be higher than 8MHz.
- To achieve 1MHz fast mode plus, the peripheral clock frequency must be higher than 20MHz.
- The above characteristic parameters of the I²C bus timing are based on: SEQ_FILTER = 01 and COMB_FILTER_En is disabled.

Figure 8 I²C Timing Diagrams



5.15 SPI Characteristics

6 Table 22 SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Master mode						
f_{SCK} ($1/t_{SCK}$)	SPI master output SCK clock frequency	Master mode SPI peripheral clock frequency f_{PCLK}	-	-	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK clock high and low time		$t_{SCK}/2 - 2$	-	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data output valid time		-	-	5	ns
$t_{H(MO)}$	Data output hold time		2	-	-	ns
$t_{SU(MI)}$	Data input setup time		5	-	-	ns
$t_{H(MI)}$	Data input hold time		5	-	-	ns
SPI Slave mode						
f_{SCK} ($1/t_{SCK}$)	SPI slave input SCK clock frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	-	-	$f_{PCLK}/3$	MHz
Duty _{SCK}	SPI slave input SCK clock duty cycle		30		70	%
$t_{SU(SEL)}$	SEL enable setup time		$3 \times t_{PCLK}$	-	-	ns
$t_{H(SEL)}$	SEL enable hold time		$2 \times t_{PCLK}$	-	-	ns
$t_{A(SO)}$	Data output access time		-	-	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data output disable time		-	-	10	ns
$t_{V(SO)}$	Data output valid time		-	-	25	ns
$t_{H(SO)}$	Data output hold time		15	-	-	ns
$t_{SU(SI)}$	Data input setup time		5	-	-	ns
$t_{H(SI)}$	Data input hold time		4	-	-	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{PCLK} = 1/f_{PCLK}$. SPI output (input) clock frequency f_{SCK} ; SPI peripheral clock frequency f_{PCLK} .

Figure 9 SPI Timing Diagrams - SPI Master Mode

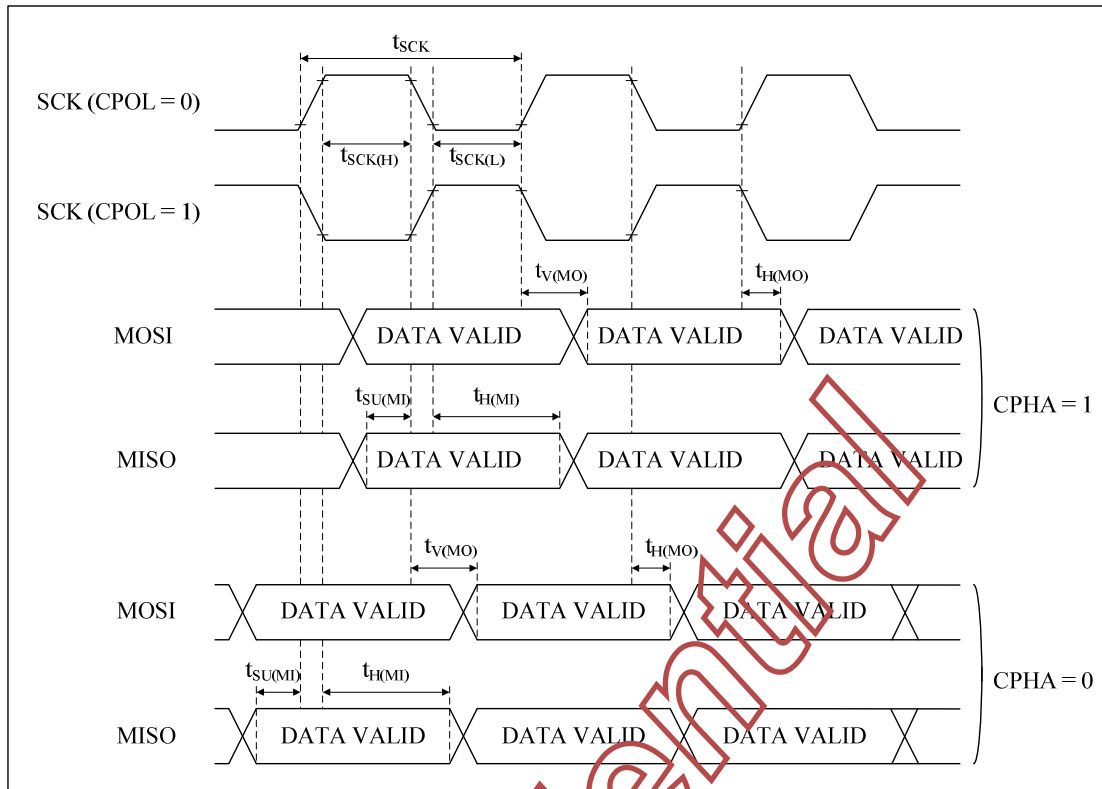
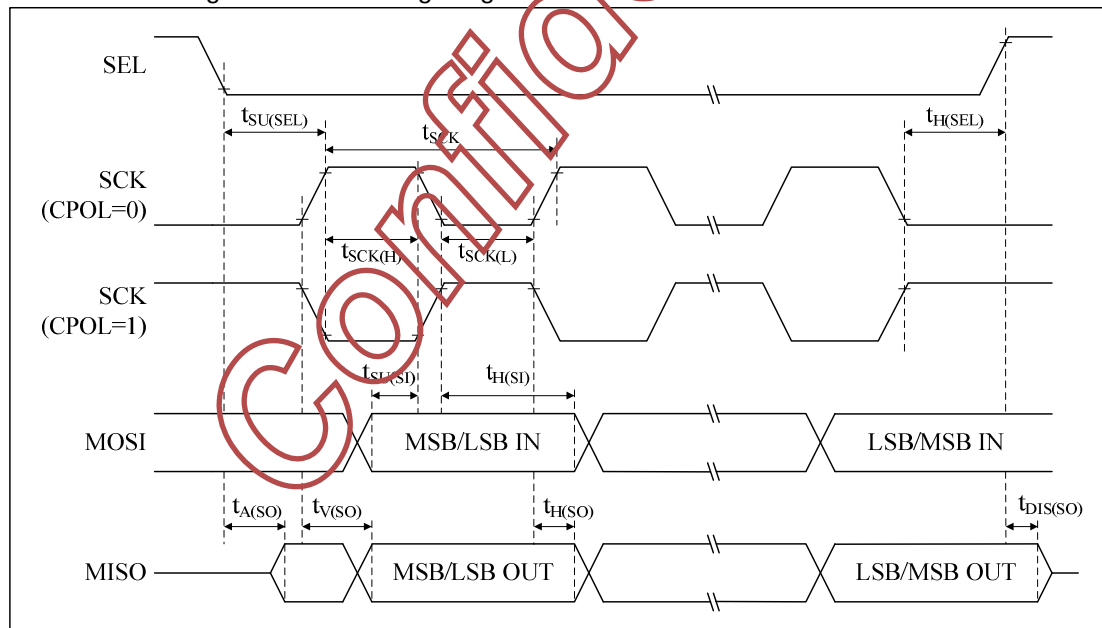


Figure 10 SPI Timing Diagrams - SPI Slave Mode with CPHA=1



6.1 I²S Characteristics

Table 23 I²S Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²S Master mode						
$t_{WSD(MO)}$	WS output to BCLK delay			TBD		ns
$t_{DOD(MO)}$	Data output to BCLK delay			TBD		ns
$t_{DIS(MI)}$	Data input setup time			TBD		ns
$t_{DIH(MI)}$	Data input hold time			TBD		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²S Slave mode						
$t_{BCH(SI)}$	BCLK high pulse width			TBD		ns
$t_{BCL(SI)}$	BCLK low pulse width			TBD		ns
$t_{WSS(SI)}$	WS input setup time			TBD		ns
$t_{DOD(SO)}$	Data output to BCLK delay			TBD		ns
$t_{DIS(SI)}$	Data input setup time			TBD		ns
$t_{DIH(SI)}$	Data input hold time			TBD		ns

Figure 11 Timing of I²S Master Mode

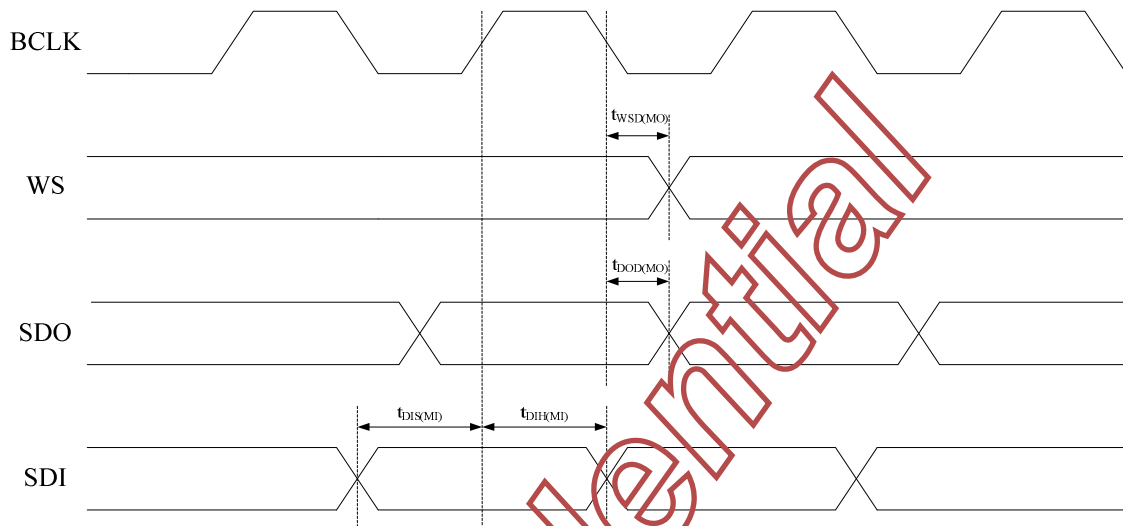
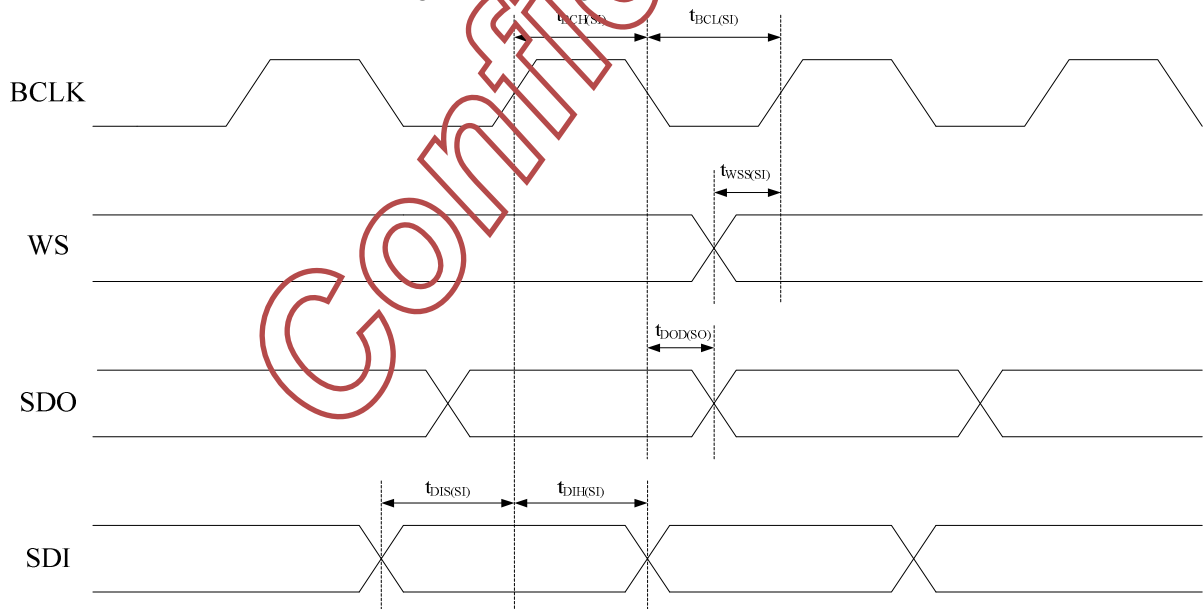


Figure 12 Timing of I²S Slave Mode



6.2 USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 24 USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	USB operating voltage		3.0	-	3.6	V
V_{DI}	Differential input sensitivity	$ USB_{DP} - USB_{DM} $	0.2	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CM}	Common mode voltage range		0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
V_{OL}	Pad output low voltage	R_L of 1.5 k Ω to V_{DD33}	0	--	0.3	V
V_{OH}	Pad output high voltage		2.8	-	3.6	V
V_{CRS}	Differential output signal cross-point voltage		1.3		2.0	V
Z_{DRV}	Driver output resistance		--	10	-	Ω
C_{IN}	Transceiver pad capacitance			-	20	pF

Note:

1. Guaranteed by design, not tested in production.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP pin should be pulled up with a 1.5 k Ω external resistor to a 3.0-to-3.6 V voltage supply.
3. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which will experience degradation in the 2.7-to-3.0 V V_{DD33} voltage range.
4. R_L is the load connected to the USB driver USBDP.

Figure 13 USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

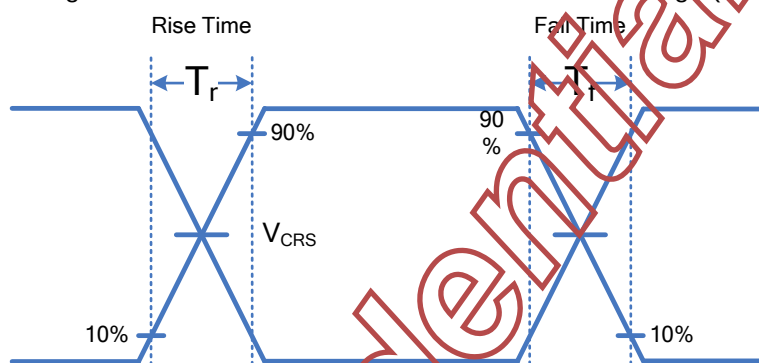


Table 25 USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_r	Rise time	$C_L = 50$ pF	4	-	20	ns
T_f	Fall time	$C_L = 50$ pF	4	-	20	ns
T_{eff}	Rise time / fall time matching	$T_{eff} = T_r / T_f$	90	-	110	%

Holtek Semiconductor Inc. (Headquarters)

No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan

Tel: 886-3-563-1999

Fax: 886-3-563-1189

<http://www.holtek.com.tw>**Holtek Semiconductor Inc. (Taipei Sales Office)**

4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan

Tel: 886-2-2655-7070

Fax: 886-2-2655-7373

Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor (China) Inc.

Building No.10, Xinzhu Court, (No.1 Headquarters), 4 Cuizhu Road, Songshan Lake, Dongguan, China 523808

Tel: 86-769-2626-1300

Fax: 86-769-2626-1311

Holtek Semiconductor (USA), Inc. (North America Sales Office)

46729 Fremont Blvd., Fremont, CA 94538, USA

Tel: 1-510-252-9880

Fax: 1-510-252-9885

<http://www.holtek.com>

Copyright © 2013 by HOLTEK SEMICONDUCTOR INC.

The information appearing in this Data Sheet is believed to be accurate at the time of publication. However, Holtek assumes no responsibility arising from the use of the specifications described. The applications mentioned herein are used solely for the purpose of illustration and Holtek makes no warranty or representation that such applications will be suitable without further modification, nor recommends the use of its products for application that may present a risk to human life due to malfunction or otherwise. Holtek's products are not authorized for use as critical components in life support devices or systems. Holtek reserves the right to alter its products without prior notification. For the most up-to-date information, please visit our web site at <http://www.holtek.com.tw>