BA45F55xx with Power Line Transceiver Application Note

D/N: AN0534EN

Introduction

A Power Line Transceiver (hereinafter referred to as “PLT”) is a fire protection dual-line bus which is used as a data transceiver. The master gives a command to the slave using a voltage signal modulation method while the slave responds to the master using a current modulation method. In this way a complete communication system between a master and slave only requires two lines. This communication method is very common in fire protection related products.

This article forms an application note for the BA45F55xx series of devices which include a PLT, providing users with a means of achieving accelerated product development.

Functional Description

Application Circuit

Figure 1 shows a PLT application circuit applied to smoke detectors. The master is connected to the slave via L1 and L2. The TRX pin receives the signal from the master. The IS pin is used to output current for data transmission. The internal structure is described in the following chapter.

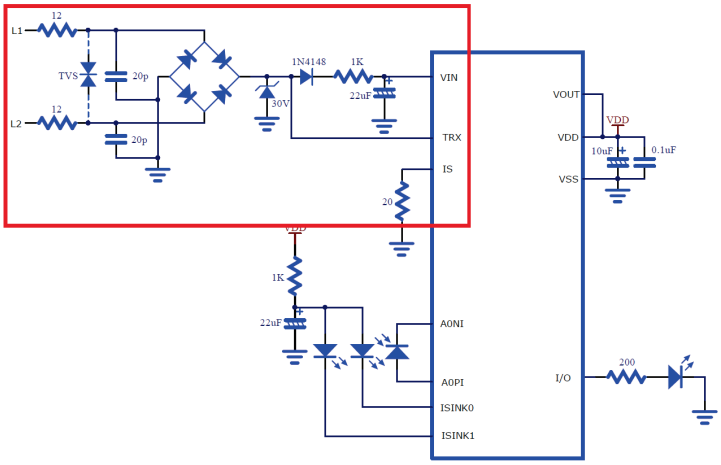

Fig. 1 Smoke Detector PLT Application Circuit

Operating Principle

Block Diagram Description

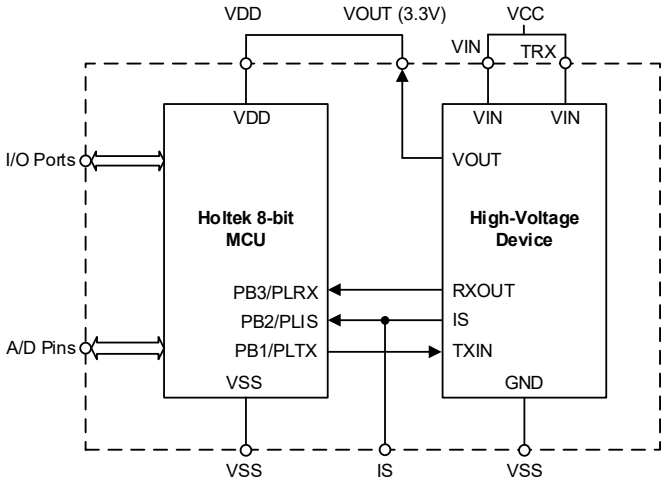

Fig. 2 MCU Block Diagram with an integrated PLT

The MCU block diagram with an integrated PLT is shown in figure 2. The bus signal is processed by the high voltage IC and then transmitted to the MCU for decoding and other relevant processing. The high voltage IC block diagram is shown in figure 3.

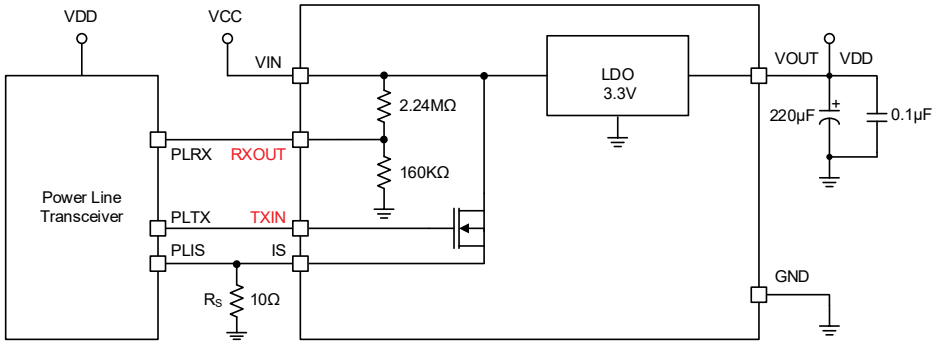

Fig. 3 High Voltage IC Block Diagram

After the power lines are connected to the high voltage IC, the RXOUT pin will transmit the power signal (1/15 of the power voltage) to the MCU for decoding. When a code needs to be transmitted to the master, this is implemented by the PLTX pin which in turn switches on the MOS.

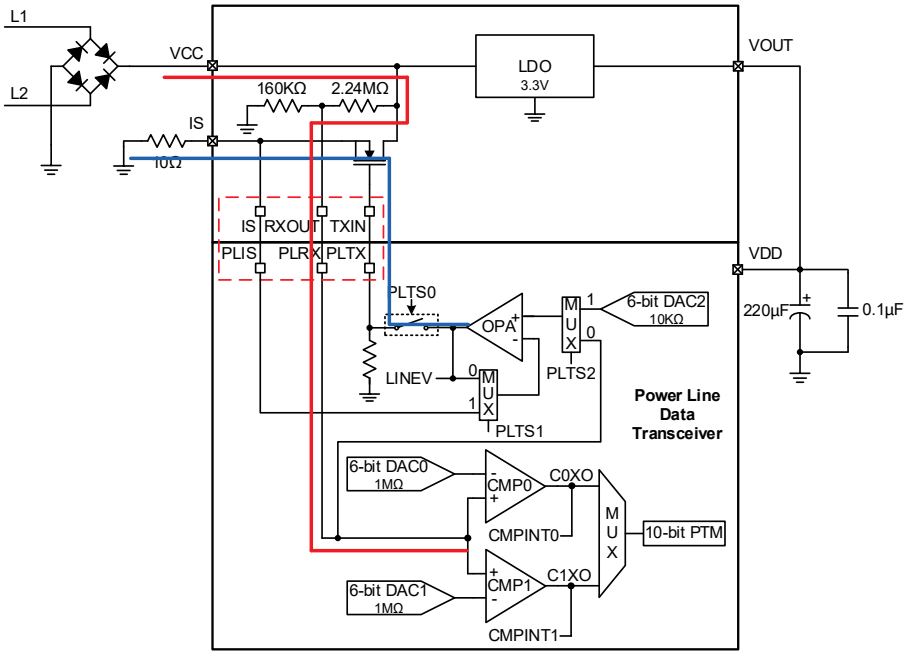

Fig. 4

As shown in the figure 4, the red line is the master transmit code path and the blue line is the slave transmit code path.

The following examples illustrate two master communication formats which allow users to set comparators according to different master formats.

- Two voltage levels：require a single comparator
- Three voltage levels：require two comparators

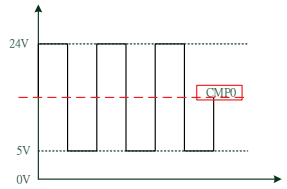

Fig. 5 Two Voltage Levels

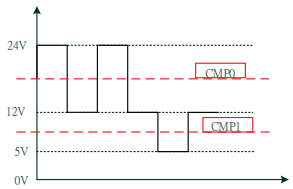

Fig. 6 Three Voltage Levels

Setting Description

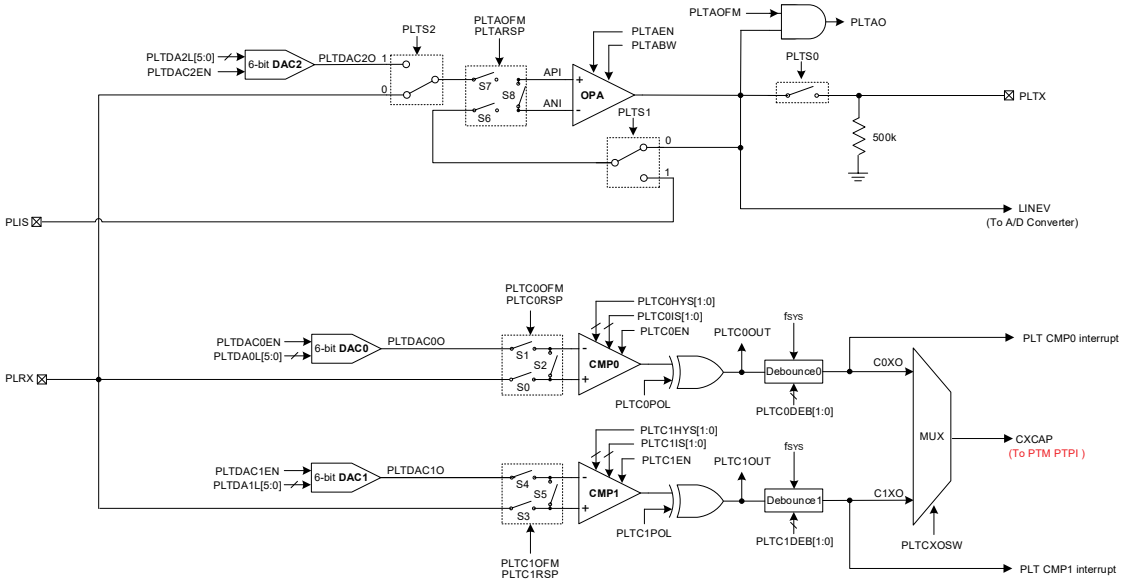

Fig. 7

The PLT is composed of two parts, one is the CMP part which is the voltage for data reception control and the other is the OPA part which is the current for data transmission control.

- Voltage for data reception control
  - The DAC0 provides a comparison base value which is controlled by the PLTDA0L[5:0]. A voltage passes through the PLRX pin to the CMP0 positive input. When this voltage is greater than DAC0, the CMP0 outputs high, otherwise it outputs Low.
  - Clear the PLTCnOFM and PLTCnRSP bits to zero. Setting these two bits only when requiring offset calibration. It is not necessary to set these two bits during normal operation.
  - PLT CMPn interrupt conditions: setting the PLTCnPOL bit high will select a falling edge to be the active interrupt edge; clearing the PLTCnPOL bit to zero will select a rising edge to be the active interrupt edge.
  - The PLTCXOSW bit is used to select the PTM capture input source which is sourced from CMP0 or CMP1.
  - In normal operation, the PTM capture input mode can be used to implement decoding.
- Current for data transmission control
  - Clear the PLTS2 bit to zero, the data transmission current is determined by DAC0.
  - Clear the PLTS1 bit to zero, this will form a Unity-gain Buffer with the high voltage IC.
  - The transmission data current is determined by the DAC2 voltage divided by the IS resistance.
  - The transmission data, whether 0 or 1 can be controlled by the PLTS0 bit.

Conclusion

This document has introduced the PLT setup method for the BA45F55xx series which can be applied to fire protection products.

Reference Material

For more details consult the Holtek website at www.holtek.com.

Version and Modification Information

Date	Author	Issue release and Modification
2019.08.13	Jia-Chieng Wu (吳嘉乾)	First version

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