

Feature

- Logic voltage : 2.7V~5.5V
- High voltage: 60V (max.)
- 3-line serial interface
- Alphanumeric and symbolic display using integrated ROM
- 24 x 8-bit display data RAM (DDRAM)
- Integrated 5x8 dot ROM containing 248 character set
- 8 user-defined characters stored in character data RAM (CGRAM)
- Additional symbol display data stored in 24 x 8-bit RAM (ADRAM)
- Display content:
24 columns by 1 row + 48 symbols - each column has 1 digit character with 2 symbols
- Supports display output: 40-segment & 24-grid
- Supports symbol output: 2-symbol & 24-grid
- Supports 2-pin general output port - static operation
- Fully integrated oscillator circuit
- 80-pin LQFP package

Applications

- Consumer products panel function control
- Industrial measuring instrument panel function control
- Other similar application panel function control
- Suitable for POS terminals or message displays

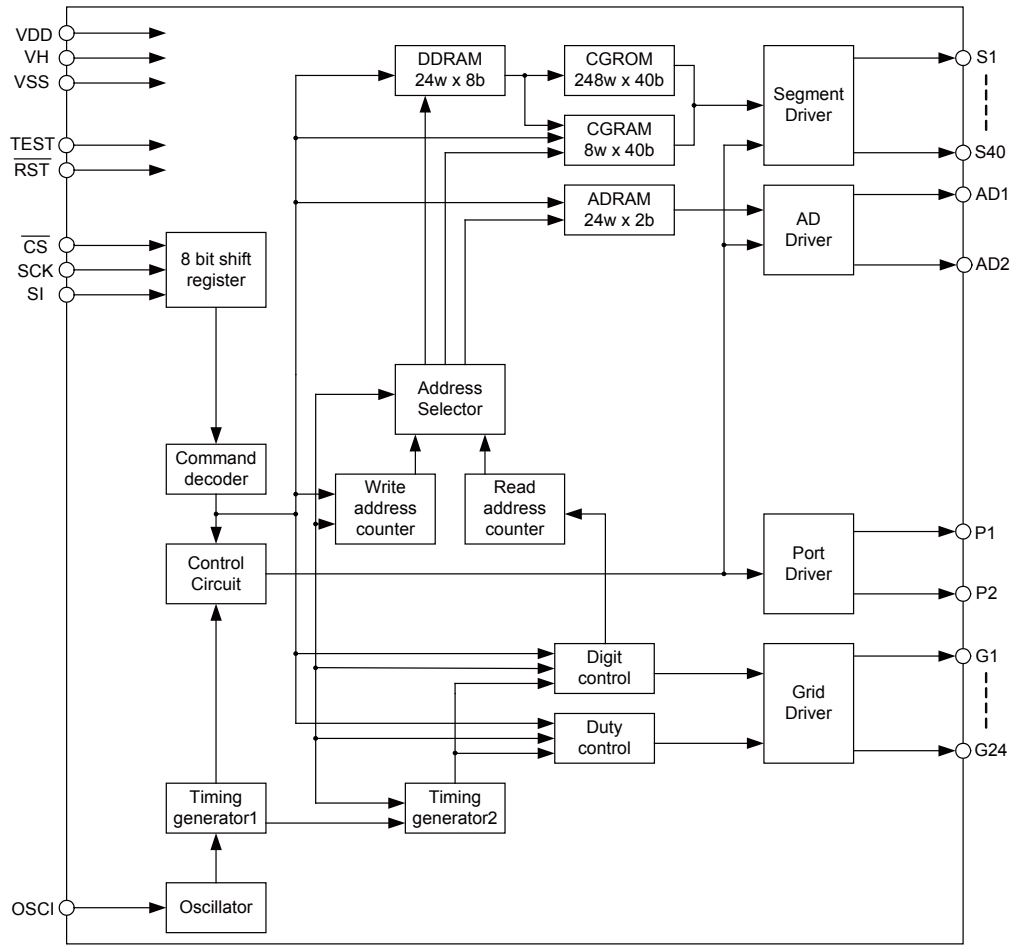
General Description

The HT16525 device is a dot matrix Vacuum Fluorescent Display, VFD, controller/driver which displays characters, numerics and symbols. Dot matrix VFD driving signals are received via a 3-line serial interface driven by an externally connected microcontroller. The display data is stored in the internal ROM and RAM for character and symbol display.

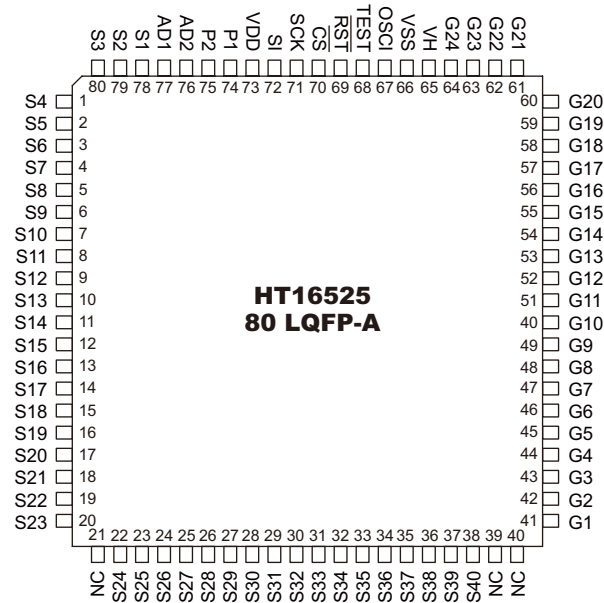
Ordering Information

| Part Number | Information |
|-------------|---------------------------------------|
| HT16525-001 | 80-pin LQFP package with ROM code 001 |
| HT16525-002 | 80-pin LQFP package with ROM code 002 |

Block Diagram



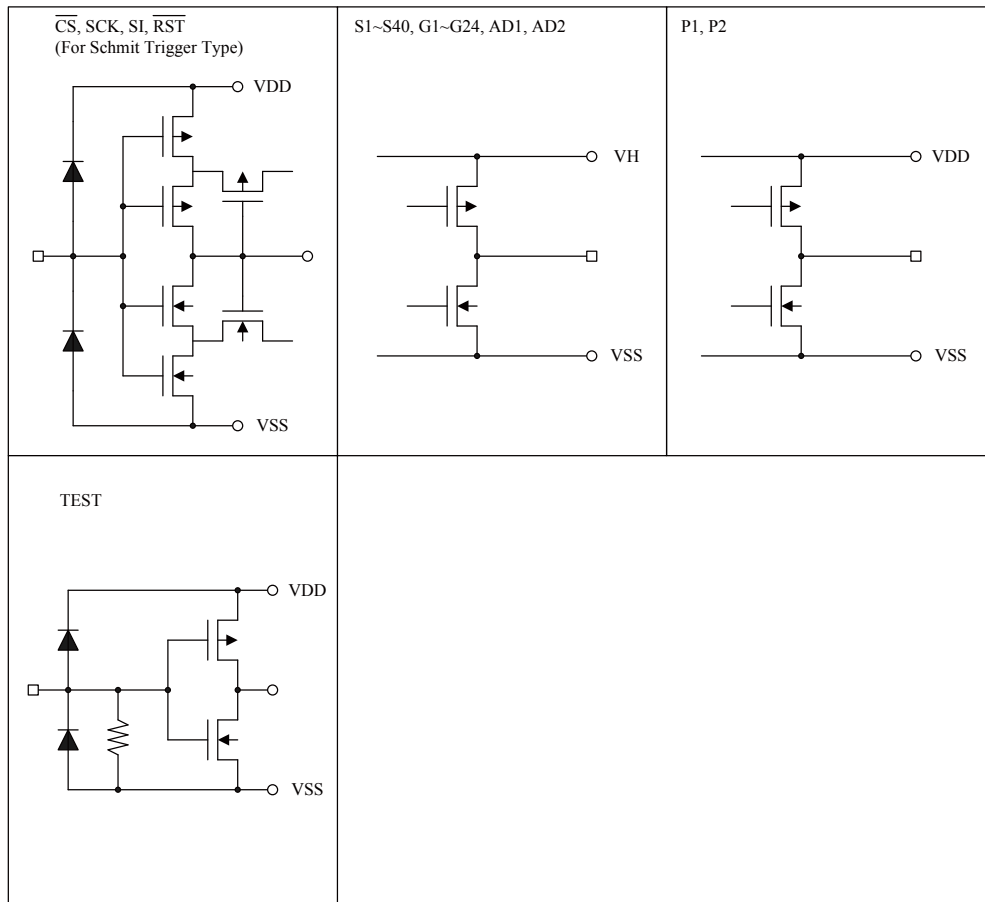
Pin Assignment



Pin Description

| Pin Name | I/O | Description |
|---------------------------------------|-----|----------------------------------------------------------------------------------------------------------------|
| Power Supply Pins | | |
| VDD | — | Positive power supply for logic circuits |
| VH | — | Power supply for VFD driver circuits |
| VSS | — | VSS - ground pin |
| Microcontroller Interface Pins | | |
| $\overline{\text{CS}}$ | I | Chip select pin When "Low", the device is active. |
| SCK | I | Serial clock input Shift clock input with data written on the SCK rising edge. |
| SI | I | Serial data input. The serial data is first shifted from LSB. |
| $\overline{\text{RST}}$ | I | Initialize all the internal registers and commands. All segments and digits are fixed at "Low" level. |
| TEST | I | When "Low" or open, the device is in normal mode. When "High", the device is in test mode. |
| Output Pins | | |
| S1~S40 | O | High-voltage segment output pins. |
| G1~G24 | O | High-voltage grid output pins. |
| AD1, AD2 | O | High-voltage additional data segment output pins. |
| P1, P2 | O | General port output. Static operation output - can drive LEDs |
| Oscillator Pin | | |
| OSC1 | I | Oscillator input pin Connected to an external resistor and capacitor to generate the oscillation frequency. |

Approximate Internal Connections



Absolute Maximum Ratings

| | | | |
|----------------------------|------------------------------------------------|----------------------------------|----------------|
| Logic Supply Voltage..... | V _{SS} -0.3V to V _{SS} +6.0V | Segment output current..... | -10mA to 4mA |
| Driver Supply Voltage..... | V _{SS} -0.3V to V _{SS} +66V | AD output current..... | -15mA to 4mA |
| Input Voltage..... | V _{SS} -0.3V to V _{DD} +0.3V | General port output current..... | -20mA to 40mA |
| Output Voltage..... | V _{SS} -0.3V to V _{DD} +0.3V | Storage Temperature..... | -55°C to 125°C |
| Grid output current..... | -20mA to 4mA | Operation Temperature..... | -40°C to 85°C |

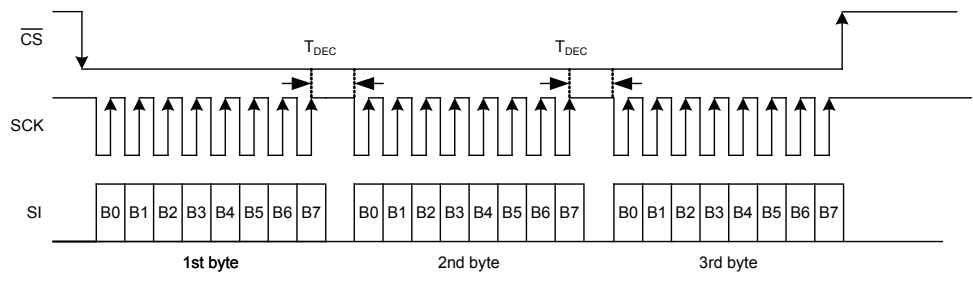
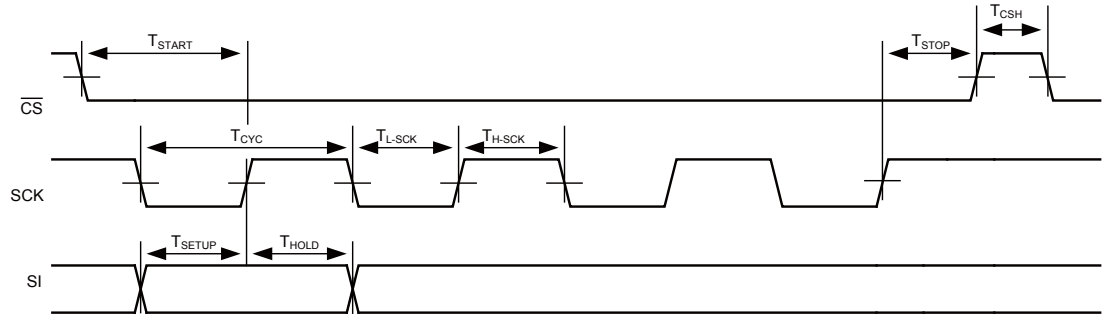
Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

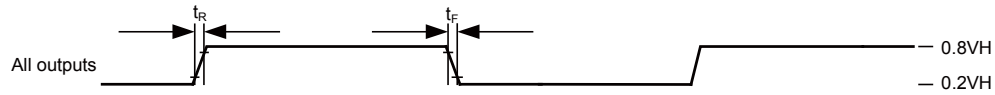
D.C. Characteristics
 $V_H=50V, V_{SS}=0V, T_a=-40^{\circ}C \sim 85^{\circ}C$

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|--------------------|---------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------|------------------------|--------------------|--------------------|------|
| | | V _{DD} | Condition | | | | |
| V _{DD} | Logic Supply Voltage | — | — | 2.7 | 5.0 | 5.5 | V |
| V _H | VFD Supply Voltage | — | — | 20 | — | 60 | V |
| I _{DD1} | VDD Operating Current | 5V | f _{osc} =2MHz, no load, Duty=15/16, Digit=1 to 24, All output lights ON, MCU no write data or command, P2 and P1=high | — | — | 2 | mA |
| | | 3V | | — | — | 1 | |
| I _{DD2} | VDD Operating Current | 5V | f _{osc} =2MHz, no load, Duty=15/16, Digit=1 to 24, Stop scan, MCU no write data or command, P2 and P1=high | — | — | 2 | mA |
| | | 3V | | — | — | 1 | |
| I _{STB} | VDD Standby Current | 5V | Standby mode | — | 2 | — | μA |
| | | 3V | | — | 2 | — | |
| I _{H1} | VH Operating Current | — | f _{osc} =2MHz, no load, Duty=15/16, Digit=1 to 24, All output lights ON, MCU no write data or command, P2 and P1=high | — | — | 1 | mA |
| I _{H2} | VH Operating Current | — | f _{osc} =2MHz, no load, Duty=15/16, Digit=1 to 24, Stop scan, MCU no write data or command, P2 and P1=high | — | — | 20 | μA |
| I _{H_STB} | VH Standby Current | — | Standby mode | — | — | 20 | μA |
| V _{IH} | High Level Input Voltage | 5V | CS, SCK, SI, RST | 0.8V _{DD} | — | — | V |
| | | 3V | | | | | |
| V _{IL} | Low Level Input Voltage | 5V | CS, SCK, SI, RST | — | — | 0.2V _{DD} | V |
| | | 3V | | | | | |
| I _{IH} | High Level Input Current | 5V | V _{IH} =V _{DD} , CS, SCK, SI, RST | — | — | 1 | μA |
| | | 3V | | | | | |
| I _{IL} | Low Level Input Current | 5V | V _{IL} =0V, CS, SCK, SI, RST | -1 | — | — | μA |
| | | 3V | | | | | |
| V _{OH1} | High Level Output Voltage | 5V | G1~G24, I _{OH1} =-15mA | 45 | — | — | V |
| | | 3V | | | | | |
| V _{OH2} | | 5V | AD1, AD2, I _{OH2} =-7mA | 46 | — | — | V |
| | | | | | | | |
| V _{OH3} | | 5V | S1~S40, I _{OH3} =-1mA | 46 | — | — | V |
| | | | | | | | |
| V _{OH4} | 5V | P1, P2 | I _{OH4} =-2mA | 0.9V _{DD} | — | — | V |
| | | | 3V | I _{OH4} =-1mA | 0.9V _{DD} | — | |
| V _{OL1} | Low Level Output Voltage | 5V | G1~G24, I _{OL1} =1mA | — | — | 5 | V |
| | | 3V | | | | | |
| V _{OL2} | | 5V | AD1, AD2, I _{OL2} =1mA | — | — | 5 | V |
| | | | | | | | |
| V _{OL3} | | 5V | S1~S40, I _{OL3} =1mA | — | — | 5 | V |
| | | | | | | | |
| V _{OL4} | 5V | P1, P2 | I _{OL4} =20mA | — | — | 1 | V |
| | | | 3V | I _{OL4} =10mA | — | — | |
| R _{PD} | Pull Down Resistor | 5V | TEST Pin | — | 50 | 100 | kΩ |
| | | 3V | | — | 100 | 200 | kΩ |

A.C. Characteristics

Serial Interface Timing

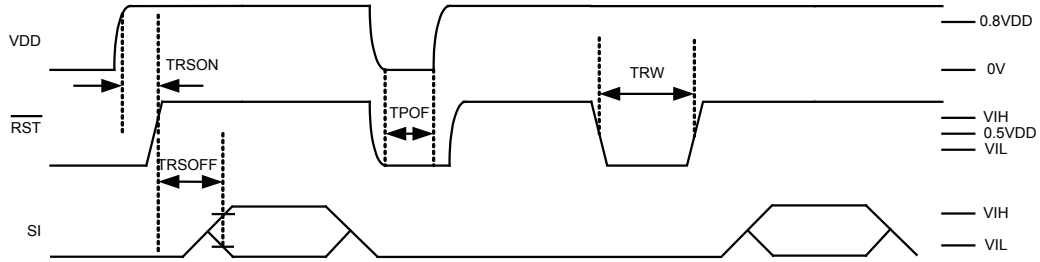


Output Timing

 $V_H=50V, V_{SS}=0V, T_a = -40^{\circ}C \sim 85^{\circ}C$

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|--------------------|--------------------------|-----------------|-------------------------------------|------|------|------|------|
| | | V _{DD} | Condition | | | | |
| f _{OSC} | Oscillation Frequency | 5V | R1=120kΩ, C1=0.1μF | 1.5 | 2 | 2.5 | MHz |
| | | 3V | | | | | |
| f _{FR} | Frame Frequency | 5V | Digit=1 to 24, R1=120kΩ, C1=0.1μF | 130 | 175 | 220 | Hz |
| | | 3V | | | | | |
| T _{CYC} | Write Cycle Time | 5V | SCK | — | — | 2 | MHz |
| | | 3V | | — | — | 2 | |
| T _{L-SCK} | Low Pulse of SCK | 5V | SCK | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{H-SCK} | High Pulse of SCK | 5V | SCK | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{SETUP} | Data Setup Time | 5V | SCK, SI | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{HOLD} | Data Hold Time | 5V | SCK, SI | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{START} | Command Start Wait Time | 5V | SCK, SI | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{STOP} | Command Stop Wait Time | 5V | SCK, \overline{CS} | 16 | — | — | μs |
| | | 3V | | 16 | — | — | |
| T _{CSH} | \overline{CS} Off Time | 5V | — | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| T _{DEC} | Command/Data Decode Time | 5V | — | 8 | — | — | μs |
| | | 3V | | 8 | — | — | |
| t _R | All Output Slew Rate | 5V | Ci=100pF, t _R =20 to 80% | — | — | 2 | μs |
| 3V | | | | | | | |
| t _F | All Output Slew Rate | 5V | Ci=100pF, t _F =80 to 20% | — | — | 2 | μs |
| 3V | | | | | | | |

Reset and Wake-up Timing

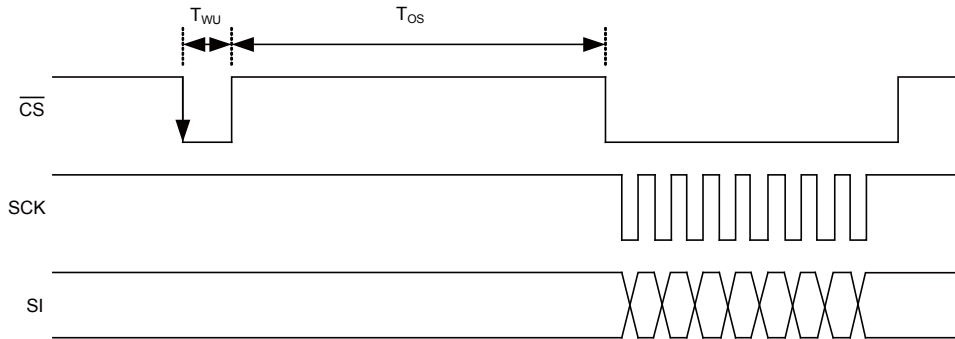
Hardware Reset



Ta=-40°C ~ 85°C

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|--------------------|------------------------|-----------------|-------------------------------------------------------------|------|------|------|------|
| | | V _{DD} | Condition | | | | |
| T _{RSON} | Oscillator Stable Time | 5V | RST signal is an external input from a microcontroller etc. | 250 | — | — | ns |
| | | 3V | | 250 | — | — | |
| | | 5V | R2=1kΩ, C2=0.1μF | — | 1000 | — | μs |
| | | 3V | | — | 1000 | — | |
| T _{POF} | VDD Off Time | 5V | VDD drop down to 0V | 40 | — | — | μs |
| | | 3V | | 10 | — | — | ms |
| T _{RW} | RST Pulse Width | 5V | RST signal is an external input from a microcontroller etc. | 400 | — | — | ns |
| | | 3V | | 400 | — | — | |
| T _{RSOFF} | SI Wait Time | 5V | — | 3 | — | — | μs |
| | | 3V | | 3 | — | — | |

Wake-up Timing

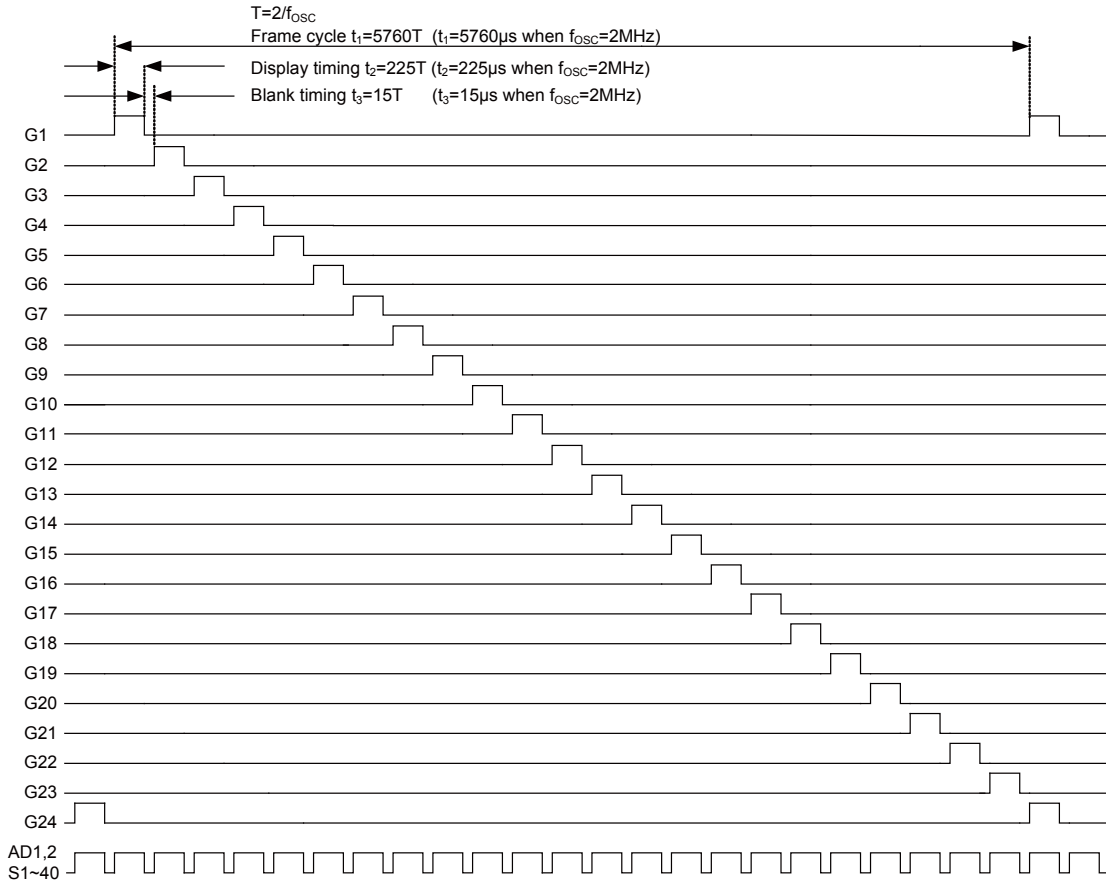


Ta=-40°C ~ 85°C

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------|-----------------|-----------|------|------|------|------|
| | | V _{DD} | Condition | | | | |
| T _{WU} | Wake-up Time | 5V | — | 200 | — | — | ns |
| | | 3V | | | | | |
| T _{OS} | Oscillation Stable Time | 5V | — | 1000 | — | — | μs |
| | | 3V | | | | | |

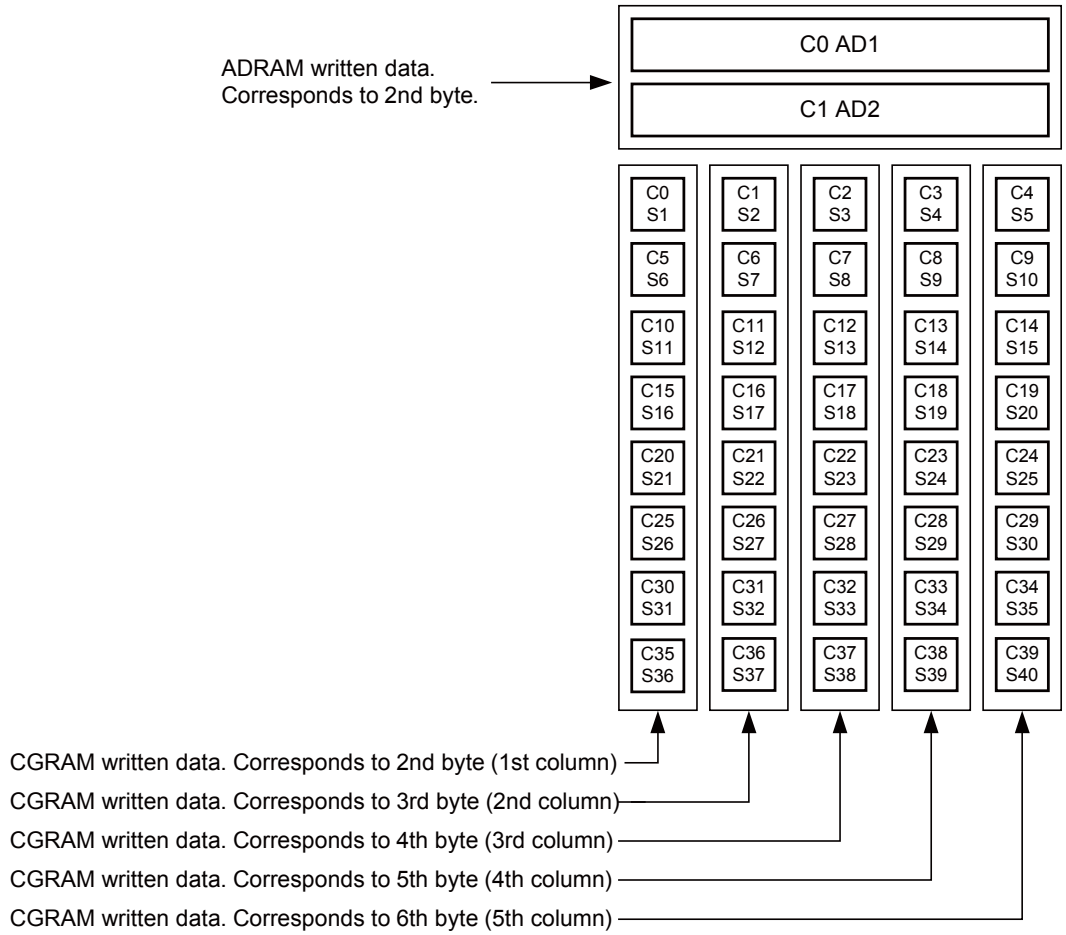
Digit Output Timing

For 24-digits display, at a duty of 15/16



Segment and AD Position

Positional relationship between S1~S40 and AD1 ~ AD2 - single digit



Command Table

| Function | Byte | R/W | Bit7 (MSB) | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (LSB) | Note | Default |
|-------------------------|------|-----|------------|------|------|------|------|------|------|------------|-------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|
| DDRAM data write | 1st | W | 0 | 0 | 0 | X4 | X3 | X2 | X1 | X0 | Xn: Address specification for each RAM | 00H |
| DDRAM data | 2nd | W | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Cn: character code specification for each RAM | — |
| CGRAM data write | 1st | W | 0 | 0 | 1 | * | * | X2 | X1 | X0 | Xn: Address specification for each RAM | 20H |
| CGRAM Data | 2nd | W | C35 | C30 | C25 | C20 | C15 | C10 | C5 | C0 | Cn: character code specification for each RAM | — |
| CGRAM Data | 3rd | W | C36 | C31 | C26 | C21 | C16 | C11 | C6 | C1 | | — |
| CGRAM Data | 4th | W | C37 | C32 | C27 | C22 | C17 | C12 | C7 | C2 | | — |
| CGRAM Data | 5th | W | C38 | C33 | C28 | C23 | C18 | C13 | C8 | C3 | | — |
| CGRAM Data | 6th | W | C39 | C34 | C29 | C24 | C19 | C14 | C9 | C4 | | — |
| ADRAM data write | 1st | W | 0 | 1 | 0 | X4 | X3 | X2 | X1 | X0 | | Xn: Address specification for each RAM |
| ADRAM Data | 2nd | W | * | * | * | * | * | * | C1 | C0 | Cn: character code specification for each RAM | — |
| General output port set | 1st | W | 0 | 1 | 1 | * | * | * | P2 | P1 | Pn: General output port status specification | 63H |
| Display duty set | 1st | W | 1 | 0 | 0 | * | * | D2 | D1 | D0 | Dn: display duty specification | 80H |
| Number of digits set | 1st | W | 1 | 0 | 1 | * | K3 | K2 | K1 | K0 | Kn: Number of digits specification | A0H |
| All lights ON/OFF | 1st | W | 1 | 1 | 0 | * | D | S | H | L | D: display on/off instruction S: standby mode instruction H: all lights ON instruction L: all lights OFF instruction | C0H |
| TEST mode | 1st | W | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | For HOLTEK internal testing | E0H |

Command and Data Transfer Methods

Complete access to the VFD driver consists of display commands and the display data. The number of the transmitted data bytes for a complete access depends upon the command and memory type as the Command Table shows. The display control commands and data are transmitted using a 3-wire serial interface from the host MCU. The following steps show how the operation of the serial interface circuitry.

- Setting the \overline{CS} pin to a “Low” level will enable a data transfer.
- Data is 8-bits wide and is sequentially shifted-in on the SI pin from LSB to MSB (LSB first)
- Data shifted into the register is ready at the rising edge of the serial shift clock SCK. If the 8-bit data is to be written in, then internal signals are automatically generated and the data will be written into the corresponding register and RAM.
- Setting the \overline{CS} pin to “High” will disable the command and data transfer
- When data is written into the RAM area including DDRAM, ADRAM and CGRAM continuously, the command used to specify the RAM area is contained in the first shifted-in command byte together with the start address. Then the RAM address will be internally incremented by 1 automatically. Therefore, it is not necessary to specify the start address of the data to be written after the command byte.

Reset Function

When the \overline{RST} pin is set to “Low”, the module is initialized to the following conditions:

- Address will be reset to 00H for each RAM including DDRAM, ADRAM and CGRAM
- The contents of the RAM including DDRAM, ADRAM and CGRAM are undefined.
- All general output ports go “High”.
- Display duty setting will be reset to 8/16 duty (register value D2, D1, D0=0, 0, 0).
- Number of digits setting will be reset to 24 digits (register value K3, K2, K1, K0=0, 0, 0, 0).
- All display lights ON/OFF settings will be switched to the “display off” mode (register value D,S,H,L=0,0,0,0)
- All segment outputs go “Low”.
- All AD outputs go “Low”.
- All grid outputs go “Low”.

Note: After a power on reset, all the RAM including DDRAM, ADRAM and CGRAM will be cleared.

Functional Description

Timing Generation Circuit

A timing generation circuit generates timing signals for the operation of internal circuits such as the DDRAM, CGRAM, CGROM and ADRAM.

VFD Driver Circuit

The VFD driver circuit consists of 24 grid signal drivers and 40 segment signal drivers. When the number of digits are selected by a corresponding command, the required grid signal drivers automatically output drive waveforms, while the other grid signal drivers continue to output non-selection waveforms. Sending serial data is latched when the display data character pattern corresponds to the last address of the display data RAM (DDRAM).

Data Display RAM - DDRAM

The Display Data RAM (DDRAM) stores the display data in 8-bit character codes. Its extended capacity is 24x8 bits or 24 characters.

DDRAM Data Write Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 0 | 0 | 0 | X4 | X3 | X2 | X1 | X0 |
| 2nd | W | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 3rd | W | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 4th | W | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| : | : | : | : | : | : | : | : | : | : |

The DDRAM data write command descriptions are shown in the following:

- X4~X0: DDRAM address is for 24 characters addressed from 00H to 17H. The addresses ranged from 18H to 1FH are unused and unavailable addresses.
- C7~C0: character code of the CGROM (internal 248 characters) or CGRAM (user-defined 8 characters)
- To specify the character code of the CGROM or CGRAM continuously, only the character code needs to be specified
- The addresses of the DDRAM are automatically incremented by 1.
- The address will be wrapped around to the start address when the DDRAM data write function is successively executed and the DDRAM address is greater than the maximum available address

- Grid positions and set DDRAM addresses

| HEX | X4 | X3 | X2 | X1 | X0 | Grid Position |
|-----|----|----|----|----|----|---------------|
| 0 | 0 | 0 | 0 | 0 | 0 | G1 |
| 1 | 0 | 0 | 0 | 0 | 1 | G2 |
| 2 | 0 | 0 | 0 | 1 | 0 | G3 |
| 3 | 0 | 0 | 0 | 1 | 1 | G4 |
| 4 | 0 | 0 | 1 | 0 | 0 | G5 |
| 5 | 0 | 0 | 1 | 0 | 1 | G6 |
| 6 | 0 | 0 | 1 | 1 | 0 | G7 |
| 7 | 0 | 0 | 1 | 1 | 1 | G8 |
| 8 | 0 | 1 | 0 | 0 | 0 | G9 |
| 9 | 0 | 1 | 0 | 0 | 1 | G10 |
| A | 0 | 1 | 0 | 1 | 0 | G11 |
| B | 0 | 1 | 0 | 1 | 1 | G12 |
| C | 0 | 1 | 1 | 0 | 0 | G13 |
| D | 0 | 1 | 1 | 0 | 1 | G14 |
| E | 0 | 1 | 1 | 1 | 0 | G15 |
| F | 0 | 1 | 1 | 1 | 1 | G16 |
| 10 | 1 | 0 | 0 | 0 | 0 | G17 |
| 11 | 1 | 0 | 0 | 0 | 1 | G18 |
| 12 | 1 | 0 | 0 | 1 | 0 | G19 |
| 13 | 1 | 0 | 0 | 1 | 1 | G20 |
| 14 | 1 | 0 | 1 | 0 | 0 | G21 |
| 15 | 1 | 0 | 1 | 0 | 1 | G22 |
| 16 | 1 | 0 | 1 | 1 | 0 | G23 |
| 17 | 1 | 0 | 1 | 1 | 1 | G24 |

Note: If the specified address in this command is not defined (X4~X0=18H~1FH), the function will not be changed.

Character Generator ROM - CGROM

- The CGROM for generating character patterns of 5x8 dots from 8-bit character codes generates 248 types of character patterns
- The character codes are shown on the following page
- Character codes 00H to 07H are allocated to the CGRAM

| MSB LSB | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|------------|--------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | RAM0 (CGRAM) | | | | | | | | | | | | | | | |
| 0001 | RAM1 (CGRAM) | | | | | | | | | | | | | | | |
| 0010 | RAM2 (CGRAM) | | | | | | | | | | | | | | | |
| 0011 | RAM3 (CGRAM) | | | | | | | | | | | | | | | |
| 0100 | RAM4 (CGRAM) | | | | | | | | | | | | | | | |
| 0101 | RAM5 (CGRAM) | | | | | | | | | | | | | | | |
| 0110 | RAM6 (CGRAM) | | | | | | | | | | | | | | | |
| 0111 | RAM7 (CGRAM) | | | | | | | | | | | | | | | |
| 1000 | | | | | | | | | | | | | | | | |
| 1001 | | | | | | | | | | | | | | | | |
| 1010 | | | | | | | | | | | | | | | | |
| 1011 | | | | | | | | | | | | | | | | |
| 1100 | | | | | | | | | | | | | | | | |
| 1101 | | | | | | | | | | | | | | | | |
| 1110 | | | | | | | | | | | | | | | | |
| 1111 | | | | | | | | | | | | | | | | |

Character Code Table for ROM Code 001

| MSB LSB | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|------------|-----------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | RAM0 (CGRAM) | | | | | | | | | | | | | | | |
| 0001 | RAM1 (CGRAM) | | | | | | | | | | | | | | | |
| 0010 | RAM2 (CGRAM) | | | | | | | | | | | | | | | |
| 0011 | RAM3 (CGRAM) | | | | | | | | | | | | | | | |
| 0100 | RAM4 (CGRAM) | | | | | | | | | | | | | | | |
| 0101 | RAM5 (CGRAM) | | | | | | | | | | | | | | | |
| 0110 | RAM6 (CGRAM) | | | | | | | | | | | | | | | |
| 0111 | RAM7 (CGRAM) | | | | | | | | | | | | | | | |
| 1000 | | | | | | | | | | | | | | | | |
| 1001 | | | | | | | | | | | | | | | | |
| 1010 | | | | | | | | | | | | | | | | |
| 1011 | | | | | | | | | | | | | | | | |
| 1100 | | | | | | | | | | | | | | | | |
| 1101 | | | | | | | | | | | | | | | | |
| 1110 | | | | | | | | | | | | | | | | |
| 1111 | | | | | | | | | | | | | | | | |

Character Code Table for ROM Code 002

Character Generator RAM - CGRAM

The CGRAM stores the pixel information (1=pixel on, 0=pixel off) for the eight user-defined 5x7 characters. Valid CGRAM addresses are 00H to 07H. Character codes 00H~07H are assigned to the user-defined characters.

CGRAM Data Write Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 0 | 0 | 1 | * | * | X2 | X1 | X0 |
| 2nd | W | C35 | C30 | C25 | C20 | C15 | C10 | C5 | C0 |
| 3rd | W | C36 | C31 | C26 | C21 | C16 | C11 | C6 | C1 |
| 4th | W | C37 | C32 | C27 | C22 | C17 | C12 | C7 | C2 |
| 5th | W | C38 | C33 | C28 | C23 | C18 | C13 | C8 | C3 |
| 6th | W | C39 | C34 | C29 | C24 | C19 | C14 | C9 | C4 |

*: Don't care

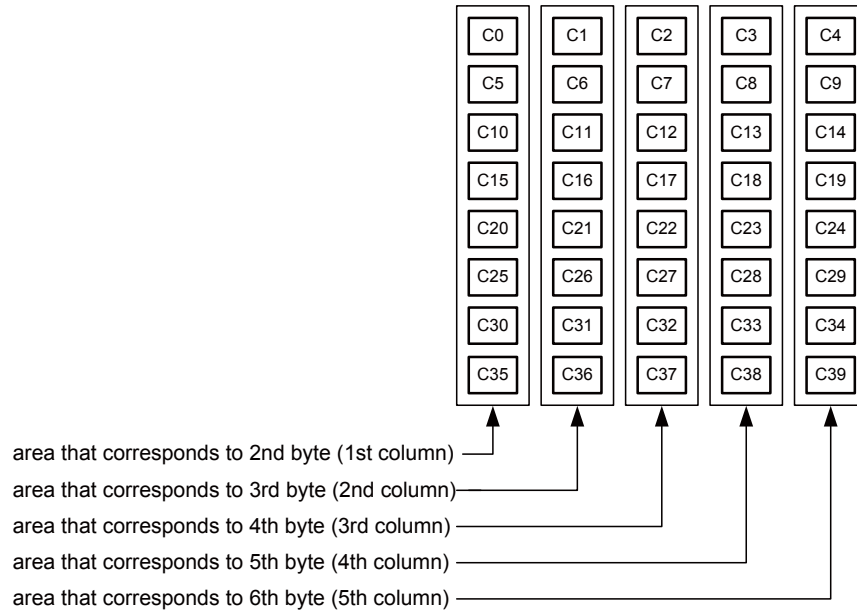
The CGRAM data write command descriptions are described by the following:

- X2~X0: CGRAM addresses for 8 user-defined characters
- C39~C0: character pattern data, 40-bit outputs per digit. The relationship between the 40-bit character pattern data and the dot positions for each digit is shown in the accompanying diagram.

- A character pattern stored in the CGRAM can be displayed and addressed by the character code specified in the DDRAM
- To specify character pattern data continuously, only the character pattern data needs to be specified
- The addresses of the CGRAM are automatically incremented by 1
- The address will be wrapped around to the start address when the CGRAM data write function is successively executed and the CGRAM address is greater than the maximum available address
- CGRAM addresses and set CGRAM addresses

| HEX | X2 | X1 | X0 | CGRAM | Mapping to CGRAM Address |
|-----|----|----|----|-------|--------------------------|
| 00 | 0 | 0 | 0 | RAM00 | 0000000B |
| 01 | 0 | 0 | 1 | RAM01 | 0000001B |
| 02 | 0 | 1 | 0 | RAM02 | 0000010B |
| 03 | 0 | 1 | 1 | RAM03 | 0000011B |
| 04 | 1 | 0 | 0 | RAM04 | 0000100B |
| 05 | 1 | 0 | 1 | RAM05 | 0000101B |
| 06 | 1 | 1 | 0 | RAM06 | 0000110B |
| 07 | 1 | 1 | 1 | RAM07 | 0000111B |

- Relationship between the CGRAM output data and the character dot position



Additional Symbol Display RAM - ADRAM

The ADRAM stores the additional symbol information (1=symbol on, 0=symbol off) for the 24 digits. For each 5x8 digit there are two symbols displayed together with the character. The positional relationship is shown in the accompanying diagram.

ADRAM Data Write Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 0 | 1 | 0 | X4 | X3 | X2 | X1 | X0 |
| 2nd | W | * | * | * | * | * | * | C1 | C0 |
| 3rd | W | * | * | * | * | * | * | C1 | C0 |
| 4th | W | * | * | * | * | * | * | C1 | C0 |
| : | : | : | : | : | : | : | : | : | : |

*: Don't care

The ADRAM data write command descriptions are described by the following:

- X4~X0: ADRAM addresses for 24 digits
- C1~C0: 2 bits Symbol data for each digit
- Symbol data specified by the ADRAM is directly output regardless of the CGRAM data and the CGROM code
- The ADRAM can store 2 types of symbol pattern for each digit
- The ADRAM contents output to the terminal can be used as a cursor for each digit
- The address of the ADRAM is automatically incremented by 1
- The address will be wrapped around to the start address when the ADRAM data write function is successively executed and the ADRAM address is greater than the maximum available address
- Grid positions and ADRAM addresses

| HEX | X4 | X3 | X2 | X1 | X0 | Grid Position |
|-----|----|----|----|----|----|---------------|
| 0 | 0 | 0 | 0 | 0 | 0 | G1 |
| 1 | 0 | 0 | 0 | 0 | 1 | G2 |
| 2 | 0 | 0 | 0 | 1 | 0 | G3 |
| 3 | 0 | 0 | 0 | 1 | 1 | G4 |
| 4 | 0 | 0 | 1 | 0 | 0 | G5 |
| 5 | 0 | 0 | 1 | 0 | 1 | G6 |
| 6 | 0 | 0 | 1 | 1 | 0 | G7 |
| 7 | 0 | 0 | 1 | 1 | 1 | G8 |
| 8 | 0 | 1 | 0 | 0 | 0 | G9 |
| 9 | 0 | 1 | 0 | 0 | 1 | G10 |

| HEX | X4 | X3 | X2 | X1 | X0 | Grid Position |
|-----|----|----|----|----|----|---------------|
| A | 0 | 1 | 0 | 1 | 0 | G11 |
| B | 0 | 1 | 0 | 1 | 1 | G12 |
| C | 0 | 1 | 1 | 0 | 0 | G13 |
| D | 0 | 1 | 1 | 0 | 1 | G14 |
| E | 0 | 1 | 1 | 1 | 0 | G15 |
| F | 0 | 1 | 1 | 1 | 1 | G16 |
| 10 | 1 | 0 | 0 | 0 | 0 | G17 |
| 11 | 1 | 0 | 0 | 0 | 1 | G18 |
| 12 | 1 | 0 | 0 | 1 | 0 | G19 |
| 13 | 1 | 0 | 0 | 1 | 1 | G20 |
| 14 | 1 | 0 | 1 | 0 | 0 | G21 |
| 15 | 1 | 0 | 1 | 0 | 1 | G22 |
| 16 | 1 | 0 | 1 | 1 | 0 | G23 |
| 17 | 1 | 0 | 1 | 1 | 1 | G24 |

Note: If the specified address in this command is not defined (X4~X0=18H~1FH), the function will not be changed.

General Output Port Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 0 | 1 | 1 | * | * | * | P2 | P1 |

*: Don't care

The general output port command descriptions are described by the following:

- P2, P1: general output port data
- The general output port supports 2-bit static output operation
- Used to control other I/O devices or controls the LEDs
- When the general output port data is set to a high level, the related pin will output a VDD level while the related pin will output a GND level when the general output port data is cleared to a low level
- Relationship between the general output port data and the output pin status

| P2 | P1 | Display State of General Output Port | Comment |
|----|----|--------------------------------------|------------------------------------------------------------------------------|
| 0 | 0 | Sets P2 to low; Sets P1 to low | — |
| 0 | 1 | Sets P2 to low; Sets P1 to high | — |
| 1 | 0 | Sets P2 to high; Sets P1 to low | — |
| 1 | 1 | Sets P2 to high; Sets P1 to high | Default state when power is applied or when the RST input is at a low level. |

Display Duty Set Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 1 | 0 | 0 | * | * | D2 | D1 | D0 |

*: Don't care

The display duty set command descriptions are described by the following:

- D2~D0: Display duty selections
- The display duty adjusts the contrast in 8 stages using 3 selection bits to adjust the pulse width of the segment output
- The relationship between the setup data and the grid duty is shown in the table.

| HEX | D2 | D1 | D0 | Grid Duty | Comment |
|-----|----|----|----|-----------|--------------------------------------------------------------------------|
| 0 | 0 | 0 | 0 | 8/16 | Default state when power is applied or when RST input is at a low level. |
| 1 | 0 | 0 | 1 | 9/16 | — |
| 2 | 0 | 1 | 0 | 10/16 | — |
| 3 | 0 | 1 | 1 | 11/16 | — |
| 4 | 1 | 0 | 0 | 12/16 | — |
| 5 | 1 | 0 | 1 | 13/16 | — |
| 6 | 1 | 1 | 0 | 14/16 | — |
| 7 | 1 | 1 | 1 | 15/16 | — |

Number of Digits Set Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 1 | 0 | 1 | * | K3 | K2 | K1 | K0 |

*: Don't care

The number of digits set command descriptions is described by the following:

- K3~K0: number of digit selections
- The number of display digits can be from 9 to 24 digits using the 4 selection bits.
- The relationship between setup data and the displayed grid is shown in the table.

| HEX | K3 | K2 | K1 | K0 | Number of Digits of Grid | Comment |
|-----|----|----|----|----|--------------------------|------------------------------------------------------------------------------|
| 0 | 0 | 0 | 0 | 0 | G1 to G24 | Default state when power is applied or when the RST input is at a low level. |
| 1 | 0 | 0 | 0 | 1 | G1 to G9 | — |
| 2 | 0 | 0 | 1 | 0 | G1 to G10 | — |
| 3 | 0 | 0 | 1 | 1 | G1 to G11 | — |
| 4 | 0 | 1 | 0 | 0 | G1 to G12 | — |
| 5 | 0 | 1 | 0 | 1 | G1 to G13 | — |
| 6 | 0 | 1 | 1 | 0 | G1 to G14 | — |
| 7 | 0 | 1 | 1 | 1 | G1 to G15 | — |
| 8 | 1 | 0 | 0 | 0 | G1 to G16 | — |
| 9 | 1 | 0 | 0 | 1 | G1 to G17 | — |
| A | 1 | 0 | 1 | 0 | G1 to G18 | — |
| B | 1 | 0 | 1 | 1 | G1 to G19 | — |
| C | 1 | 1 | 0 | 0 | G1 to G20 | — |
| D | 1 | 1 | 0 | 1 | G1 to G21 | — |
| E | 1 | 1 | 1 | 0 | G1 to G22 | — |
| F | 1 | 1 | 1 | 1 | G1 to G23 | — |

All Display Lights On/Off Set Command

| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 1 | 1 | 0 | * | D | S | H | L |

*: Don't care

The display ON/OFF set command descriptions are described by the following:

- S bit: S="1" is standby mode; S="0" is normal mode
- D bit: D="1" is display ON; D="0" is display OFF
- H bit: set all lights ON
- L bit: set all lights OFF
- When S bit = "1", the internal oscillator stops and all outputs are set to low and the general port is set to high (P2 and P1 are all at high levels)
- When S bit = "1", all registers will keep their original value
- After being woken up, the device will set the S and D bits to "0"
- The "All display lights ON" command is used primarily for display testing
- The "All display lights OFF" command is primarily used for display flashing
- The command bits, including D, H and L bits, can not control the general output port
- The relationship between the control bits and display state of G1~G24, S1~S40 and AD1~AD2 pins is shown in the table.

| D | S | H | L | Driver Output Status | Comment |
|---|---|---|---|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| 1 | 0 | 0 | 0 | Normal display | — |
| 1 | 0 | 0 | 1 | Sets all segments and AD to Low All grids keep scan General ports active | — |
| 1 | 0 | 1 | * | Sets all segments and AD to High All grids keep scan General ports active | — |
| 0 | 0 | * | * | Sets all segments and AD to Low Sets all grids to Low General ports active | Display off mode (Default state when power is applied or when the RST input is at a low level.) |
| * | 1 | * | * | Sets all segments and AD to Low Sets all grids to Low Set General ports to high | Standby mode |

*: Don't care

Wake-up Setting

The wake-up behavior is described by the following:

- The device is woken up when a \overline{CS} low pulse is asserted i.e. when a \overline{CS} signal falling edge occurs.
- The D and S control bits described in the preceding section will be set to “0” - display off mode
- The oscillator starts to oscillate after wake-up
- The VFD driver does not display until the host MCU transmits commands to it.



TEST Command

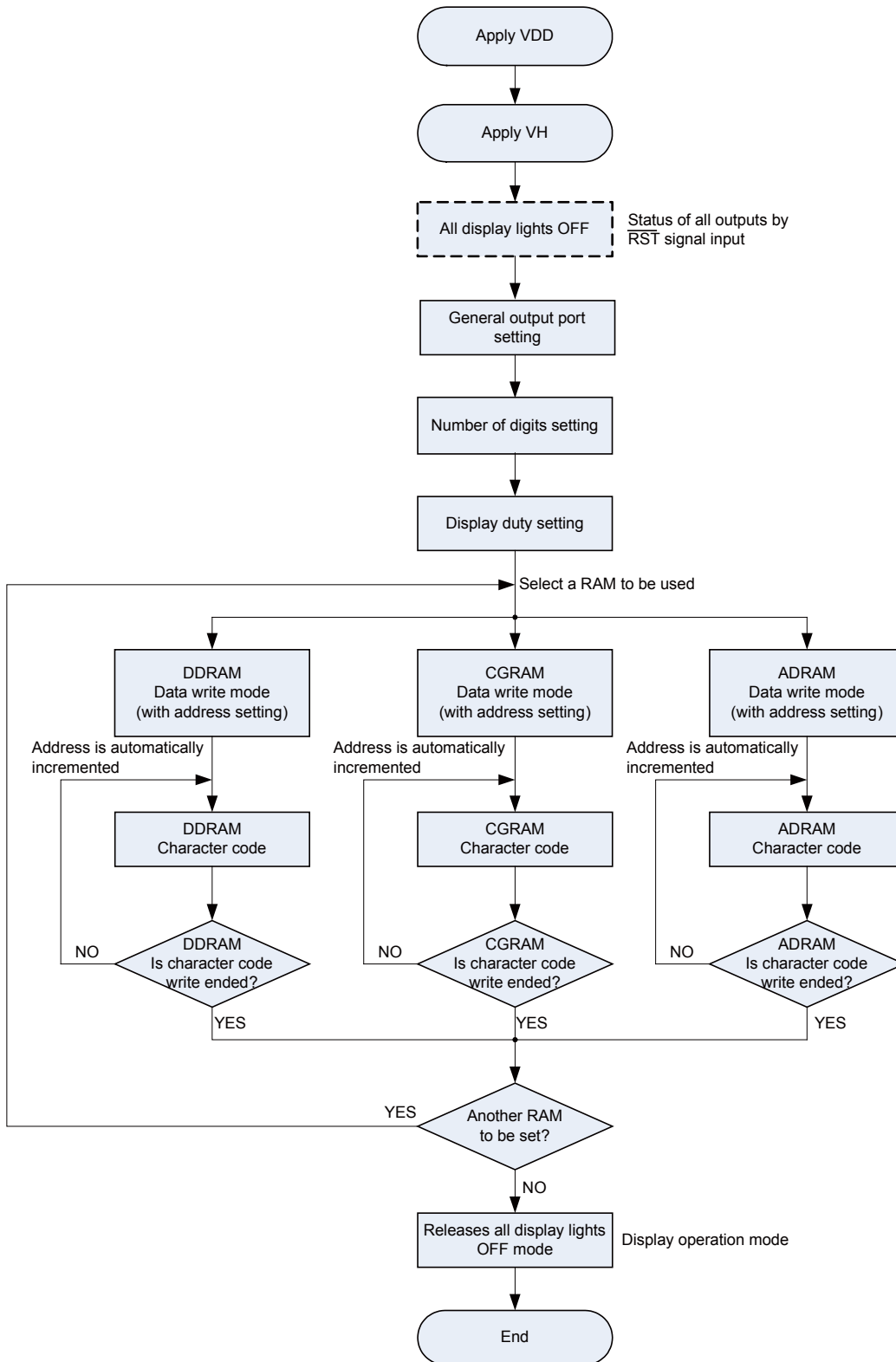
| Byte | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|-----|------|------|------|------|------|------|------|------|
| 1st | W | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

The TEST command is described by the following:

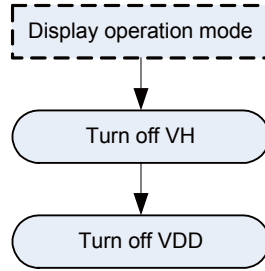
- Only when the TEST pin is high is the TEST command “E0H” is valid
- This command is used by HOLTEK for internal testing.

Setting Flowchart

Power Applied Included

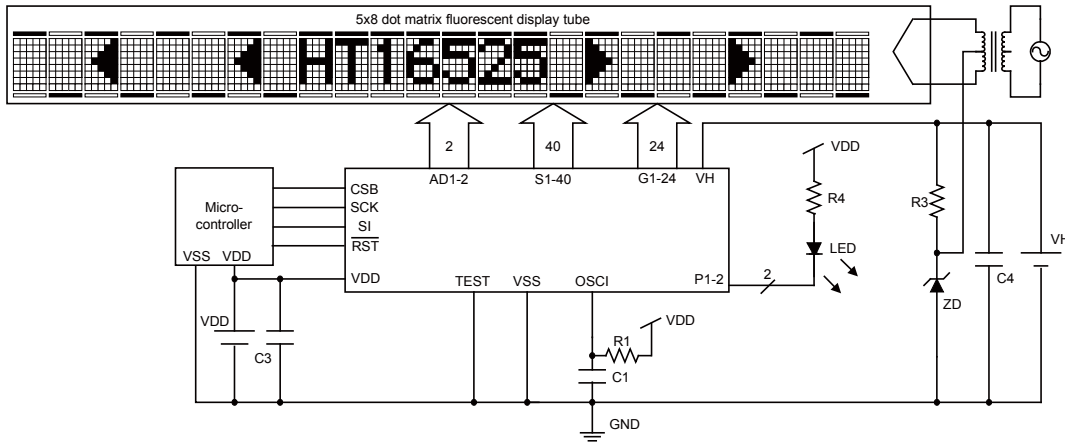


Power-off Flowchart

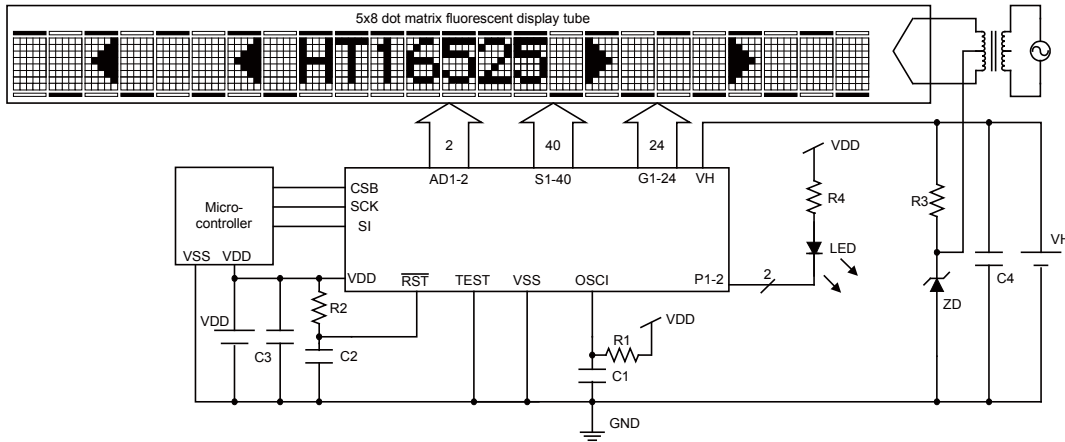


Application Circuit

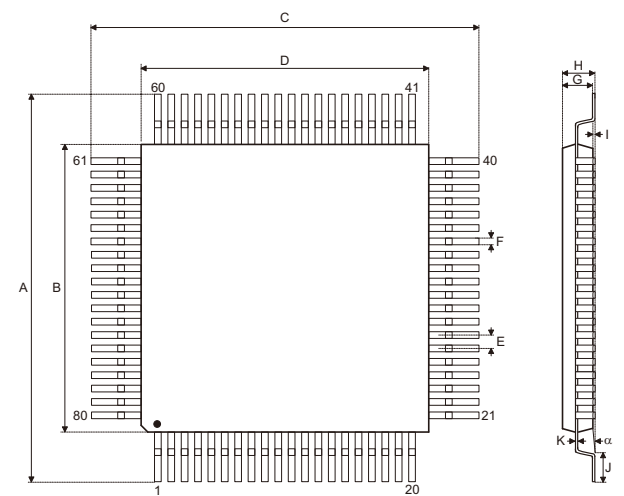
RST Pin is Connected to a MCU



RST Pin is Connected to External Resistor and Capacitor



- Note: 1. The VDD value depends on the power supply voltage of the microcontroller used. Adjust the values of the components R2, R4, C2, C3 and C4 according to the power supply voltage used.
2. The VH value depends on the fluorescent display tube used. Adjust the values of the components R3 and ZD according to the power supply voltage used.
3. R1=120kΩ, C1=0.1μF.

Package Information
80-pin LQFP (10mmx10mm) Outline Dimensions


| Symbol | Dimensions in inch | | |
|----------|--------------------|-------|-------|
| | Min. | Nom. | Max. |
| A | 0.469 | — | 0.476 |
| B | 0.390 | — | 0.398 |
| C | 0.469 | — | 0.476 |
| D | 0.390 | — | 0.398 |
| E | — | 0.016 | — |
| F | — | 0.006 | — |
| G | 0.053 | — | 0.057 |
| H | — | — | 0.063 |
| I | — | 0.004 | — |
| J | 0.018 | — | 0.030 |
| K | 0.004 | — | 0.008 |
| α | 0° | — | 7° |

| Symbol | Dimensions in mm | | |
|----------|------------------|------|-------|
| | Min. | Nom. | Max. |
| A | 11.90 | — | 12.10 |
| B | 9.90 | — | 10.10 |
| C | 11.90 | — | 12.10 |
| D | 9.90 | — | 10.10 |
| E | — | 0.40 | — |
| F | — | 0.16 | — |
| G | 1.35 | — | 1.45 |
| H | — | — | 1.60 |
| I | — | 0.10 | — |
| J | 0.45 | — | 0.75 |
| K | 0.10 | — | 0.20 |
| α | 0° | — | 7° |

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