

Using the PFD Function in the HT47R20A-1

D/N : HA0036E

Introduction

This application shows how to use the PFD function in the HT47R20A-1 MCU device.

The HT47R20A-1 pin, PA3, has a dual function. In addition to being a normal I/O pin, this pin can also function as a PFD (Programmable Frequency Divider) output. The required function, whether normal I/O pin or PFD pin, is selected via a configuration option.

After the configuration option has chosen the PFD function, when the program sets the value of pin PA3 to a "0" (CLR PA.3) the waveform will appear on the PFD output. If PA3 is set as a "1" (SET PA.3) then pin PA3 will remain at a low level. The source clock for the PFD is controlled by the timer/event counter overflow signal.

PA3	Functional Description
0 (CLR PA.3)	PA3=PFD output
1 (SET PA.3)	PA3=0

PFD Output Frequency = $(1/2) \times (1/\text{timer overflow period})$

By using the above formula, the maximum output frequency is given by setting the initial timer value to 0FFFFH, therefore if the clock source is the system frequency, which is 480kHz, then the PFD output frequency will be 240kHz.

Using the PFD Function

- Configuration options
PFD enable: The PA3 option should be selected to be a PFD output
- Software
The PFD output frequency is dependent upon the timer/event counter overflow period. Therefore by setting up different values of timer/event counter preset values, different frequencies for the PFD can also be setup.

For example, to obtain a 1kHz waveform the PFD frequency formula is:

$$f_{PFD} = (1/2) \times (1/\text{timer-event counter overflow period})$$

$$\text{Timer/Event counter overflow period} = 0.5\text{ms}$$

$$\text{Timer/Event counter preset value} = 0.0005 \times 480000 = 240$$

- Program:


```
include ht47r20a-1.inc
data .section 'data'
code .section at 0 'code'
    org    00h
    jmp   start
;-----
    org    20h
start:
    clr   intc0
    clr   intc1
    clr   adcr.1           ;Enable Timer/Event Counter
    mov   a,08h           ;Timer/Event Counter Source Clock
                                ; setup as the System clock
    mov   tmrc,a          ;Setup preset value
    mov   a,low(65536-240) ;low byte value shown by ( )
    mov   tmrbl,a
    mov   a,high(65536-240); high byte value shown by ( )
    mov   tmrbh,a
    clr   pa.3            ;enable the PFD output
    set   tmrc.4          ;start the timer/event counter
    jmp   $
```