

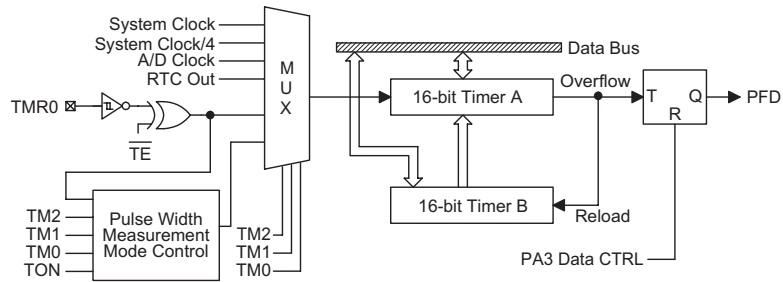
Using the Timer/Event Counter in the HT47R20A-1

D/N : HA0031E

Introduction

The following notes introduce the usage of the HT47R20A-1 Timer/Event Counter.

The HT47R20A-1 has a 16 bit continuous counting timer/counter known as TMRAH, TMRAL and TMRBH, TMRBL. TMRAH and TMRAL are used for counting and TMRBH, TMRBL are preload registers for storing the timer/counter initial value. The timer/counter initial value should first be written to low bit and then to high bit like from TMRAL, TMRBL to TMRAH and TMRBH. The clock source of the timer/counter can be the system clock, instruction clock (system clock/4) and RTC clock. See the timer/event counter structure as shown in the figure below:



TMRC is the timer/counter control register which defines the operating mode, counting enable/disable and trigger. See the description below:

Name	Bit	Function Description
—	0~2	Undefined, read as "0"
TE	3	Defines timer/counter TMR function edge (0=rising edge, 1=falling edge)
TON	4	Enable/disable the timer counter (0=disable, 1=enable)
		Defines the operating method (TM2, TM1, TM0)
		000=counter mode (system clock)
		001=counter mode (system clock/4)
TM0	5	010=counter mode (RTC output)
TM1	6	011=A/D counter mode (RC oscillator determined by the ADCR register)
TM2	7	100=counter mode (external clock)
		101=pulse width detect mode (system clock/4)
		110=no definition
		111=no definition

TMRC Register

TM0, TM1 and TM2 define the counter mode which is used for internal clock counting. The clock source is derived from the internal clock. The counter mode functions as an external counter and its clock source is the TMR input. The A/D counter mode functions as external A/D input counter (as for the A/D conversion, refer to other introductions). In the pulse width measurement mode, counting operation can be done at a high or low level of the external TMR pin. The clock source is the instruction clock.

In the timer mode, A/D counter mode or counter mode, once the timer/counter starts counting, namely from the current value (TMRAH and TMRAL to FFFFH, if an overflow occurs, the counter will preload to the register TMRBH and TMRBL) of the timer/counter to preload the value already loaded into the preload register, and set the bit interrupt request flag (TF; fourth bit of the INTC1).

In the pulse width measurement mode, when the TON and TE bit value is "1" and if the TMR receives a transient signal from low to high level (or from high to low level if the TE bit value is "0"), the counter will start counting until the TMR pin returns to its original level and clear the TON bit to "0". The measured result will remain in the timer/counter such that only one pulse width can be counted at a time. When the TON bit is reset as "1", once the TMR receives a PWM pulse, the counting continues. In the pulse width measurement mode, the timer/counter starts counting not according to the logic level but according to the transient edges. Once an overflow occurs, the counter will reload the register initial value from the timer/counter and send an interrupt request just like the timer/counter mode.

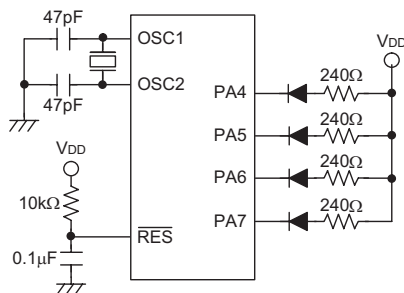
Set the counter start bit (TON; the fourth bit of TMRC) as "1" to start the counter. In pulse width measurement mode, TON bit will be cleared after the cycle is measured. It can only be cleared by instruction in the other three modes. The timer/counter overflow can be used as wake-up signal or set as a PFD output by options. No matter what the operation mode is, writing a "0" to ETI bit can disable the corresponding interrupt service.

If the timer/counter is off, data written to the timer/counter register will be reloaded to the timer/counter. However, if the timer/counter is turned on, data written to it will only be kept in the timer/counter register. The timer/counter will not be changed and will go on counting until an overflow occurs to reload the new initial value in the register.

The clock will be blocked to avoid errors when reading the timer/counter data. As clock blocking may result in a counting error, this must be taken into consideration by the programmer.

The Usage of Timer/Event Counter

Hardware: PA4~PA7 pins are individually connected to the LED as shown below.



→ Timer Mode

When the timer/counter operates in the timer mode, the clock source can be selected by instructions as system clock, instruction clock (system clock/4) or real time clock overflow signal (selected by softwares.)

Clock Source	Frequency
System Clock	480kHz
Instruction Clock	120kHz
Real Time Clock	32768Hz

- Program List

```

;File Name: timer1.asm
;Description: using the timer mode
include ht47r20a-1.inc
data .section 'data'
int_count db ?           ;interrupt counting register
io_count  db ?           ;I/O status register
code .section at 0 'code'
    org 00h
    jmp start
    org 04h
    reti
    org 08h
    reti
    org 0ch
    reti
    org 10h
    jmp timer_int        ;timer/counter interrupt input
;-----
    org 20h
start:
    clr intc0
    clr intc1
    clr adcr.1
    set tmrc.5           ;set instruction clock as counter
                        ;clock (120kHz)

    mov a,0ah
    mov int_count,a
    clr io_count
    mov a,LOW(65536-12000); timer/counter initial value
    mov tmral,a         ;interrupt occurs at 0.1 second
    mov tmrb1,a
    mov a,HIGH(65536-12000)
    mov tmrah,a
    mov tmrbh,a
    set tmrc.4          ;start timer/counter
    set intc1.0
    set intc0.0
    jmp $
;-----
timer_int:
    sdz int_count      ;determine if the interrupts have
                        ;exceeded 10 times
    reti              ;below 10 times, return to inc
    io_count          ;over 10 times, io_count incremented
                        ;by 1
    swapa io_count     ;show the result through the LED
    cpl acc

```

```

mov    pa,a
mov    a,0ah                ;int_count is restarted again
mov    int_count,a
reti

```

- Program Description

The timer interrupt occurs every 0.1 second and counting will be recorded by the int_count. When the counting reaches 10 times (equals to 1 second,) the io_count will be incremented by "1" and shown through the LED. With 4 LEDs in binary format, the maximum time it can be shown is 16 seconds.

→ **Counter Mode**

When the timer/counter operates in the counter mode, the clock source is the external TMR input signal.

- Program List

```

;File Name: timer2.asm
;Description: using the external counter mode
include ht47r20a-1.inc
data .section 'data'
count    db ?                ;counter register
code .section at 0 'code'
    org    00h
    jmp    start
    org    04h
    reti
    org    08h
    reti
    org    0ch
    reti
    org    10h
    jmp    timer_int        ;timer/counter interrupt
;-----
start:
    clr    intc0
    clr    intc1
    clr    adcr.1            ;timer/counter enable
    set    tmrc.7            ;count the external clock
    clr    count
    mov    a,LOW(65536-1000);timer/counter initial value
    mov    tmral,a           ;count 1000 external events and
                                ;interrupt that occurs

    mov    tmrbl,a
    mov    a,High(65536-1000)
    mov    tmrah,a
    mov    tmrbh,a

```

```

set   tmrc.4           ;start the timer/counter
set   intc1.0         ;timer/counter interrupt enable
set   intc0.0         ;all interrupt enable
jmp   $
;-----
timer_int:
inc   count           ;interrupt is incremented by 1
swapa count          ;show the result through the LED
cpl  acc
mov  pa,a
reti

```

- Program Description

Timer/counter interrupt occurs each time the external event counting reaches 1000 and shows the number through the LED. With 4 LEDs, the interrupts can be shown 16 times in binary format up to a maximum of 1600 times of external events.

→ **Pulse Width Measurement Mode**

Pulse width measurement mode can measure the transition time between high and low levels from the external input signals.

- Program List

```

;File Name: timer3.asm
;Description: using the pulse width measurement mode
include ht47r20a-1.inc
data .section 'data'
count db ?           ;interrupt counter register
code .section at 0 'code'
org 00h
jmp start
org 04h
reti
org 08h
reti
org 0ch
reti
org 10h
jmp timer_int       ;timer/counter interrupt
;-----
start:
clr  intc0
clr  intc1
clr  adcr.1
set  tmrc.5         ;pulse width measurement mode, clock
                        ;source is the instruction clock
set  tmrc.7
clr  count

```

```
mov a,Low(65536-60000);timer/counter initial value
mov tmral,a           ;interrupt occurs at every 0.5 second
mov tmrbl,a
mov a,High(65536-60000)
mov tmrah,a
mov tmrbh,a
set tmrc.4
set intc1.0
set intc0.0
jmp $
;-----
timer_int:
inc count             ;interrupt is incremented by 1
swapa count          ;the result is shown through the LED
cpl acc
mov pa,a
reti
```

- Program Description

In the pulse width measurement mode, timer/counter interrupt occurs at every 0.5 second and the result will be displayed through the LED. With 4 LEDs in binary format, the interrupt display can be shown 16 times in all and up to 8 seconds of pulse width.