

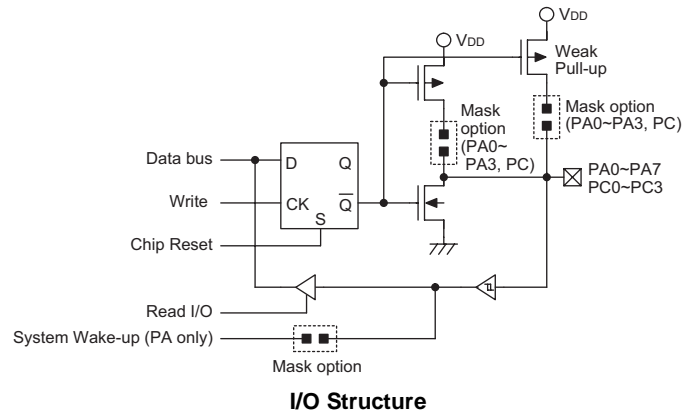
# Using the I/Os in the HT49 MCU Series

D/N : HA0026E

## Introduction

In the HT49C30-1/HT49R30A devices there are 8 bi-directional I/O pins on PA and 6 input pins on PB. In the HT49C50-1/T49R50A-1 devices there are 12 bi-directional I/O pins composed of 8 pins on PA and 4 pins on PC, as well as 8 input pins on PB. In the HT49C70-1/T49R70A-1 there are 16 bi-directional pins, composed of 8 pins on PA and 8 pins on PC as well as 8 input pins on PB. PA, PB and PC have the Data Memory addresses of [12H], [14H] and [16H] respectively. In the Configuration Options, PA and PC can be selected to be either NMOS or CMOS types and can have pull-high resistors connected.

If the PA and PC structures NMOS types, then before reading data, it is necessary to write a "1" to the related pin to turn off the corresponding NMOS device and to enable the pin to operate as an input. In other words, first use the "SET [m].i" instruction to switch of the related NMOS device, then use the "MOV A, [m]" instruction to read the data.

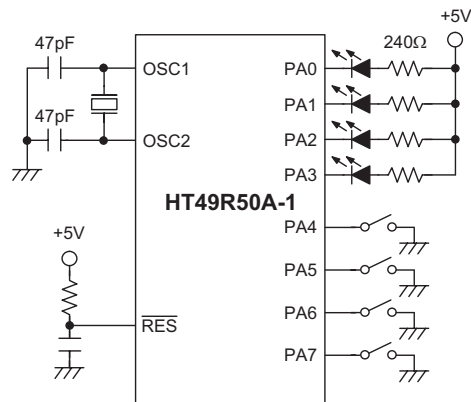


Some bit control instructions are of a "Read-modify-write" type which first read the value on the pins. In these bit control instructions, during this read process, the value of all the pins on the port are read, after which the value of the related bit is modified, and then the value rewritten back to the output data latch. Because of this process, the original value of some bits in the output latch may be inadvertently changed, and as a result output the wrong value. For example, for the instructions "SET [m].i", "CLR [m].i", "CPL[m]" and "CPLA[m]", will all first read the value of the port into the CPU, after which the related bit will be modified and the resulting value written back to the output data latch or the accumulator. Therefore, for I/O pins, which are setup in an input condition, when these bit control instructions are executed, the value of the internal latch may be changed. Therefore care must be exercised when using these instructions.

### Program Example

- Configuration Options  
For PA0~PA3, choose CMOS structures with pull-high resistors.
- Hardware  
PA0~PA3 are connected to LEDs, PA4~PA7 are connected to switches

#### Application Circuit



- Program Description  
As shown in the diagram above, PA0~PA3 are used as outputs and PA4~PA7 used as inputs. The program is used to read the condition on the switches into the MCU, then interchanging the read back value onto the PA0~PA3 pins to show the position of the switches. In this way the illuminated LEDs will show the condition of each related switch.

**Program Statements**

```
-----  
;FILE NAME : IO.asm  
;Author : Au  
;Objective : Show the I/O function of the HT49 series  
;;  
-----  
include ht49r50a-1.inc  
code .section 'code'  
    org     00h  
    jmp     start  
    org     20h  
start:  
    mov     a,0ffh  
    mov     pa,a           ;setup as inputs  
    mov     a,pa          ;read switch status  
    swap    acc            ;exchange 4 low bits with 4 high bits  
    mov     pa,a          ;output data to LEDs  
    jmp     start  
end
```

- Configuration Options  
PC selected to have CMOS structures with pull high resistors
- Hardware  
PA7 and PA0 are connected
- Program Description  
The objective of the program is to show how execution of "read-write-modify" instructions can create some special conditions.

### Program Statements

```

;-----
;FILE NAME : rmw.asm
;Author : Ruan Qin
;Objective : show how to use the "read-modify-write" instruction
;Hardware connections : PA7 and PA0 are connected together
;;;
include ht49r50a-1.inc
code .section at 0 'code'
      org      00h
      jmp      start
;-----

      org      20h
start:                                ;PA7(latch value) pin value,
                                      ;PA0(latch value) pin value

      clr      pa                      ; (0)0 , (0)0
      set      PA7                      ; (1) ; (1)0 , (0)0
      set      PA0                      ; (2) ; (0)0 , (1)0
      ;set     PA7                      ; (3)
      sz      PA7
      jmp      r_1
r_0:
      jmp      $
r_1:
      jmp      $

```

- Program Description

For details consult the program statement comments. When executing the above program, it is discovered that the value on the PA0 and PA7 pins is always 0, but actually the internal latch value of PA0 and PA7 has changed. Check the program notes for details.

If single stepping is used to run, the "Read-modify-write" process. When the program has finished executing (2), break the connection between PA0 and PA7, then when executing the following instruction it will be found that PA0 has changed to a value of "1."

If statement (3) is added, then after (2) has finished executing, it will be found that PA0 = 1 and PA7 = 1. If the program is run until statement (3) has finished it will be found that PA0=0 and PA7=1. It is important that these differences are understood when using the "read-modify-write" instructions.

For all of the NMOS structures, if they are to be used as inputs, then a "1" must first be written to the pin, before the input status of the same pin is read. Each time an NMOS port pin is to be read, the read instruction must always be preceded by writing a "1" to the same pin, to eliminate the possibility of creating errors when executing "read-modify-write" instructions.