

Watchdog Timer Setup for the HT49 MCU

D/N : HA0008E

Introduction

In the MCU application, a watchdog timer is provided to prevent software malfunction or sequences from jumping to unknown locations with unpredictable results. In the program if WDT is not cleared after a certain period of time, the WDT will overflow and the system will reset. With HT49R50A-1 as an example, this Application Note introduces the Watchdog Timer Setup for the HT49 series MCU

Operating Description

In the HT49R50A-1, there are three kinds of WDT clock source: system clock/4, RTC OSC and WDT OSC. The WDT clock source can originate from the instruction clock or system clock frequency divided by four. The clock source in crystal mode is 455K~4000K. In RC mode, when $V_{DD}=3V$ the clock source is 400K~2000K, and 400K~3000K when $V_{DD}=5V$. The WDT clock can also be supplied by a 32768Hz RTC OSC (real time clock oscillator), or by its own internal 12kHz WDT OSC (WDT oscillator).

When one of the three sources of frequency f_s is selected, the HT49R50A-1 passes through a 16-stage divider, and the WDT overflow frequency is at a minimum at $f_s/2^{15}$. To execute the "CLR WDT" instruction, the clear instruction only resets the last stage of the divider chain. The exact division ratio depends upon the residual value in the watchdog timer counter before the clear instruction is executed. If all is set as "1", the device only needs to pass through a 15-stage divider for the WDT to overflow. Therefore, the HT49R50A-1 WDT overflow frequency is between $f_s/2^{15}$ ~ $f_s/2^{14}$.

Supposing the overflow frequency is $f_s/2^{15}$, then the overflow period is $2^{15}/f_s$. The following table shows the clock source and overflow period:

Clock Source	Overflow Period
WDT OSC : 12kHz	$2^{15}/12000=2.73S$
RTC OSC : 32768Hz	$2^{15}/32768=1S$
System clock : 455kHz	$2^{15}/(455000/4)=0.288S$
System clock : 1M	$2^{15}/(1000000/4)=0.131S$
System clock : 2M	$2^{15}/(2000000/4)=0.0655S$
System clock : 4M	$2^{15}/(4000000/4)=0.0327S$

Note: 1K=1000

1M=1000,000

In HALT mode, the system clock will stop, if the system clock is chosen as the WDT clock source then the WDT will also stop. If the WDT OSC or RTC OSC is chosen as the WDT clock source, then in HALT mode the watchdog won't stop working. Therefore, if it is necessary to employ WDT function in power saving mode, choose WDT OSC or RTC OSC as the clock source. Under electromagnetic interference or if the device operates in a noisy environment, using the internal WDT OSC or RTC OSC is strongly recommended.

When in WDT OSC mode, the WDT time out period will vary with temperature, voltage and process variations. The WDT will be cleared under the following three conditions: The first is a system reset, the second is via "HALT" instruction or when the system enters a power down mode and the third is via software instruction. There are two options of using software instructions to clear the contents of the Watchdog Timer, one of which must be chosen by configuration option. The first option is to use the single "CLR WDT" instruction while the second is to use the two commands "CLR WDT1" with "CLR WDT2" (for more information, refer to other Application Notes with detailed explanations).