

# Using the HT16C21 in Audio Panel Applications

D/N : HA0290E

## Introduction

The HT16C21 is an LCD driver device. It has multiple display modes (Max: 20×4 or 16×8). This application uses the HT68F30 as the master MCU to control an audio panel LCD Display and uses the HT16C21 driving function for a 20×4 LCD. The purpose of the application is to allow users to grasp the characteristics and applications of the HT16C21 more clearly.

## Operation Features

### HT16C21 Features

- Operating voltage: 2.4V~5.5V
- Internal 32kHz RC oscillator
- Bias: 1/3 or 1/4
- Duty: 1/4 or 1/8
- Support I<sup>2</sup>C interface
- Two Selectable LCD frame frequencies: 80Hz or 160Hz
- Versatile blinking modes (OFF/0.5Hz/1Hz/2Hz)
- R/W address auto increment
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Low power consumption ( $V_{DD} = 3V$ ,  $I_{DD} = 18\mu A$ ,  $I_{STB} = 1\mu A$ )
- Multiple Display Patterns:
  - For 1/4 Duty: Maximum Display Dots: 20 Segments × 4 Commons
  - For 1/8 Duty: Maximum Display Dots: 16 Segments × 8 Commons
- Package Type: 20/24/28-pin SOP and 16-pin NSOP

## Operating Principle

### Display RAM Structure

The HT16C21 contains a 16×8 bits display RAM to store the LCD display data. Writing a “1” means the related LCD segment is on. Writing a “0” means the related LCD segment is off.

For 1/4 duty: the LCD Pattern and its corresponding Display RAM Mapping are shown in the accompanying table:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
SEG13					SEG12					06H
SEG15					SEG14					07H
SEG17					SEG16					08H
SEG19					SEG18					09H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

Figure 1 20×4 Display Mode RAM Mapping

For 1/8 duty: the LCD Pattern and its corresponding Display RAM Mapping are shown in the accompanying table:

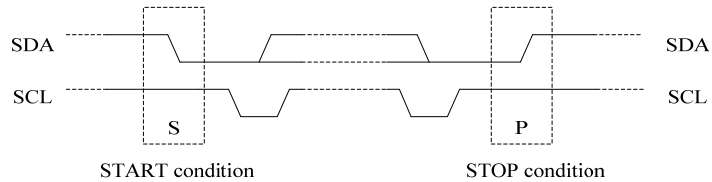
Output	COM7/SEG3	COM2/SEG2	COM1/SEG1	COM0/SEG0	COM3	COM2	COM1	COM0	Address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
SEG10									06H
SEG11									07H
SEG12									08H
SEG13									09H
SEG14									0AH
SEG15									0BH
SEG16									0CH
SEG17									0DH
SEG18									0EH
SEG19									0FH
	D7	D6	D5	D4	D3	D2	D1	D0	Data

Figure 2 16×8 Display Mode RAM Mapping

**HT16C21 Communication Method**

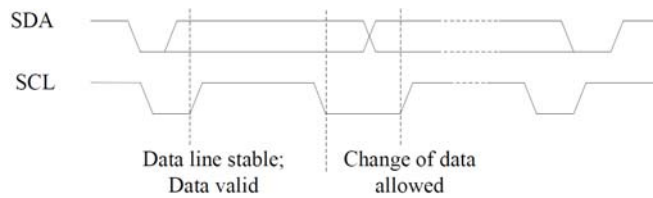
The HT16C21 drives the LCD via the I<sup>2</sup>C interface.

- I<sup>2</sup>C START signal and STOP signal  
 When the SCL line remains high, a START condition occurs when a high to low transition on the SDA line takes place. A STOP condition occurs when a low to high transition on the SDA line takes place as shown in Figure 3.



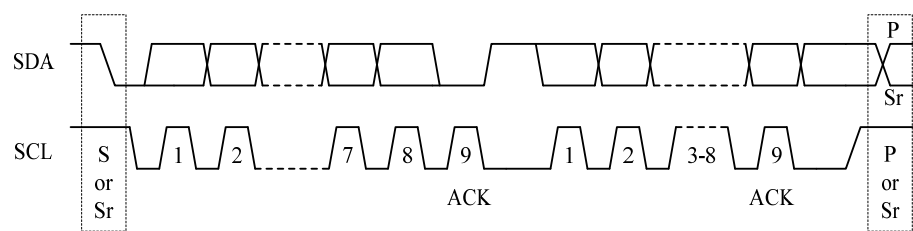
**Figure 3 Start and Stop Condition**

- I<sup>2</sup>C communication data operation  
 During data transfer, when SCL is high, the SDA data is valid. When SCL is low, the SDA data changes as shown in figure 4.



**Figure 4 Data Validity**

- Byte transmission in the I<sup>2</sup>C communication  
 There must be an acknowledge signal after a data byte is transmitted by the I<sup>2</sup>C. When the acknowledge signal is "0", transmission will continue. When the signal is "1", transmission stops.



**Figure 5 Byte Format**

- I<sup>2</sup>C Communication Write Operation

For the HT16C21 the write operation is shown below. A byte write operation always requires a Start signal, a 7-bit slave address and a read/write flag (0: write, 1: read). A Command Byte Write operation, then requires a command byte, a command setting byte and a stop signal. A Data Byte Write Operation, requires a command byte, a Register address byte, a data byte and a stop signal.

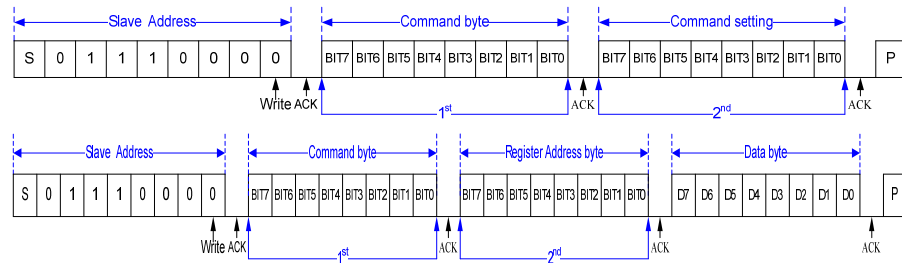


Figure 6 Command Byte Write Operating

- Page Write Operation

For a successive data write operation, after completing writing a data byte, the address pointer will be increased by 1 automatically for a write operation to the next address. When the internal address pointer reaches the maximum Display RAM address, the address pointer will be reset to 00H as shown in figure 7 below.

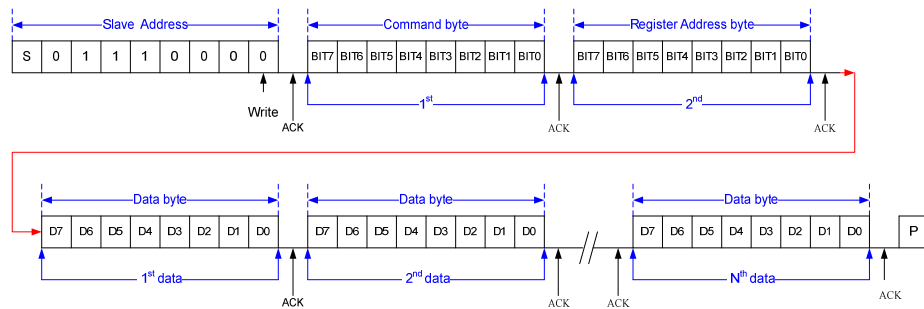
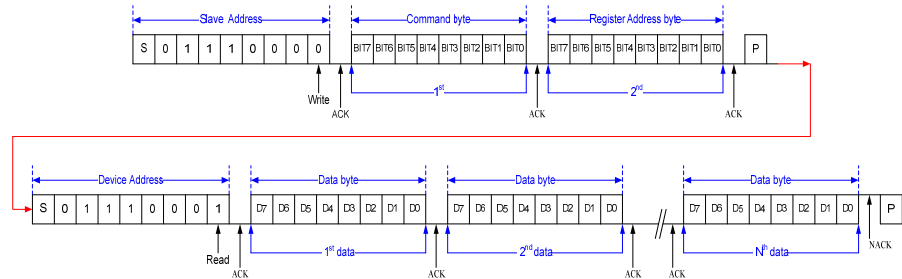


Figure 7 Page Write Operation

- I<sup>2</sup>C Communication Read Operation

The read operation is shown in figure 8 below. A byte read operation requires a Start signal, a 7-bit slave address, a read/write flag, a command byte and a Register address byte. The slave will send data to the host. After receiving a data byte, the address pointer will be incremented by 1 for a read operation to the next address.



**Figure 8 Read Operating**

### HT16C21 Command Summary

- Display Data Input Command

This command is used for the MCU to send data to the HT16C21 Display RAM.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Display data input/output command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	X	X	A3	A2	A1	A0	Display data start address of memory map	W	00H

Power on status: Address is set 00H.  
If the programmed command is not defined, the function will not be affected.

- Drive Mode Command

This command is used to set the HT16C21 Drive mode.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Driver mode setting command	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias setting	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Note:

Bit		Duty	Bias
Duty	Bias		
0	0	1/4duty	1/3bias
0	1	1/4duty	1/4bias
1	0	1/8duty	1/3bias
1	1	1/8duty	1/4bias

Power on status: The drive mode 1/4 duty output and 1/3 bias is selected.  
If the programmed command is not defined, the function will not be affected.

- System Mode Command

This command is used to control the Display and Internal RC oscillator.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/off Setting	2nd	X	X	X	X	X	X	S	E		W	00H

Note:

Bit		Internal System oscillator	LCD Display
S	E		
0	X	Off	Off
1	0	On	Off
1	1	On	On

Power on status: Display and Internal RC oscillator are off.  
If the programmed command is not defined, the function will not be affected.

• Frame Frequency Command

This command is used to select the LCD Frame frequency.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Note:

Bit	Frame Frequency
F	80Hz
1	160Hz

Power on status: Frame frequency is set to 80Hz.  
If the programmed command is not defined, the function will not be affected.

• Blinking Frequency Command

This command is used to select the LCD Blinking Frequency.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Blinking Frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking Frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Note:

Bit	Blinking Frequency
BK1 BK0	
0 0	Blinking off
1 1	2Hz
1 0	1Hz
0 1	0.5Hz

Power on status: LCD Blinking is off.  
If the programmed command is not defined, the function will not be affected.

• Internal Voltage Adjustment (IVA) Setting Command

This command is used to select the Segment and VLCD pin-shared function and enable/disable the internal voltage adjustment function.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Internal Voltage Adjustment (IVA) Setting	1st	1	0	0	0	1	0	1	0		W	
Internal Voltage Adjust control	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	<ul style="list-style-type: none"> <li>The Segment/VLCD shared pin can be programmed via the "DE" bit.</li> <li>The "VE" bit is used to enable or disable the internal voltage adjustment for bias voltage.</li> <li>The DA3-DA0 bits can be used to adjust the VLCD output voltage.</li> </ul>	W	30H

Note:

Bit		Segment / VLCD shared pin select	Internal Voltage Adjustment	Note
DE	VE			
0	0	VLCD pin	Off	<ul style="list-style-type: none"> <li>The Segment/VLCD pin is set as the VLCD pin.</li> <li>Disable the internal voltage adjustment function.</li> <li>One external resistor must be connected between VLCD pin and VDD pin to determine the bias voltage, and internal voltage follower (OP4) must be enabled by setting the DA3-DA0 bits as the value other than "0000".</li> <li>If the VLCD pin is connected to the VDD pin, the internal voltage follower (OP4) must be disabled by setting the DA3-DA0 bits as "0000".</li> </ul>
0	1	VLCD pin	on	<ul style="list-style-type: none"> <li>The Segment/VLCD pin is set as the VLCD pin.</li> <li>Enable the internal voltage adjustment function.</li> <li>The VLCD pin is an output pin of which the voltage can be detected by the external MCU host.</li> </ul>
1	0	Segment pin	Off	<ul style="list-style-type: none"> <li>The Segment/VLCD pin is set as the Segment pin.</li> <li>Disable the internal voltage adjustment function.</li> <li>The bias voltage is supplied by the internal VDD power.</li> <li>The internal voltage-follower (OP4) is disabled automatically and DA3-DA0 don't care.</li> </ul>
1	1	Segment pin	On	<ul style="list-style-type: none"> <li>The Segment/VLCD pin is set as the Segment pin.</li> <li>Enable the internal voltage adjustment function.</li> </ul>

Power on status: Enable the internal voltage adjustment function; The Segment/VLCD pin is set as the Segment pin.  
If the programmed command is not defined, the function will not be affected.

**HT16C21 Operating Flow Chart**

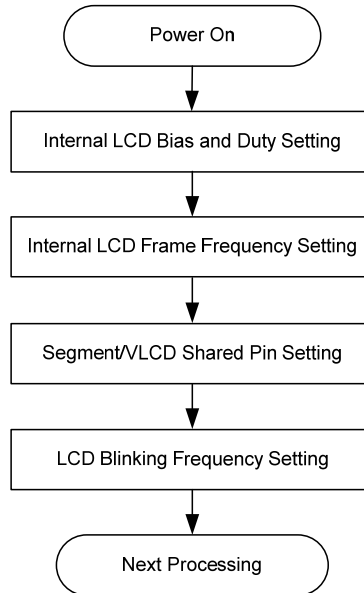
After power on, the MCU must initialise the LCD. The following steps achieve this:

Step 1: Set the internal LCD Bias and Duty.

Step 2: Set the internal LCD Frame Frequency

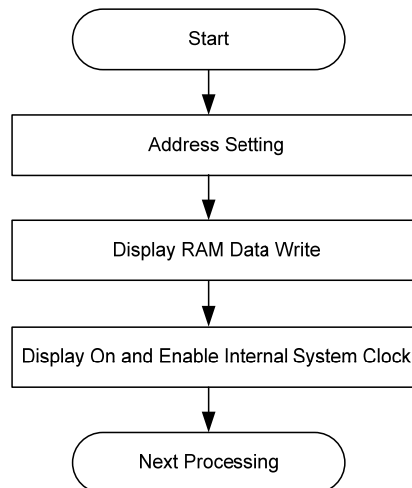
Step 3: Set the VLCD/Segment Shared pin

Step 4: Set the LCD Blinking Frequency



**Figure 9 HT16C21 Initialisation**

The HT16C21 Display flowchart is shown below. First set the RAM Address, then write the Display RAM Data and finally enable the Internal System Clock and turn on the LCD Display.



**Figure 10 Display Data Read/Write**

## LCD Panel

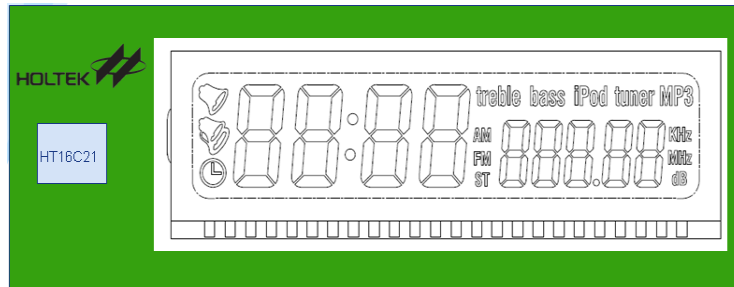


Figure 11 LCD Panel

Figure 11 shows the Audio LCD Panel. Parameter Summary: 1/4 duty, 1/3 bias, Operating Voltage 3.0V. The displayed content has the following meaning:

- |                                   |                      |
|-----------------------------------|----------------------|
| 1. treble: treble                 | 2. bass: bass        |
| 3. ipod: ipod mode                | 4. tuner: Radio Mode |
| 5. MP3: MP3 mode                  | 6. FM/AM: FM/AM      |
| 7.  : alarm 1                     | 8.  : alarm 2        |
| 9. <b>ST</b> : stereo/single-tone | 10.  : current time  |

## Application Circuit Diagram

The complete system consists of both a Top Board and a Lower Board, as shown in Figure 12 and Figure 13 respectively.

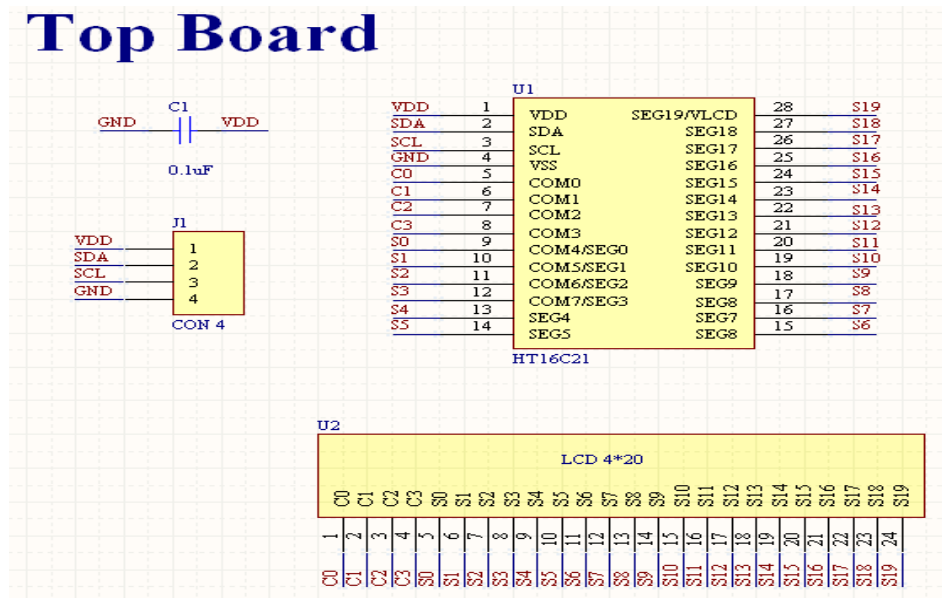


Figure 12 Top Board Application Circuit

Top Board: LCD Driver IC -- HT16C21, audio LCD Panel and CON4 interface used for I<sup>2</sup>C communication with the Bottom Board.

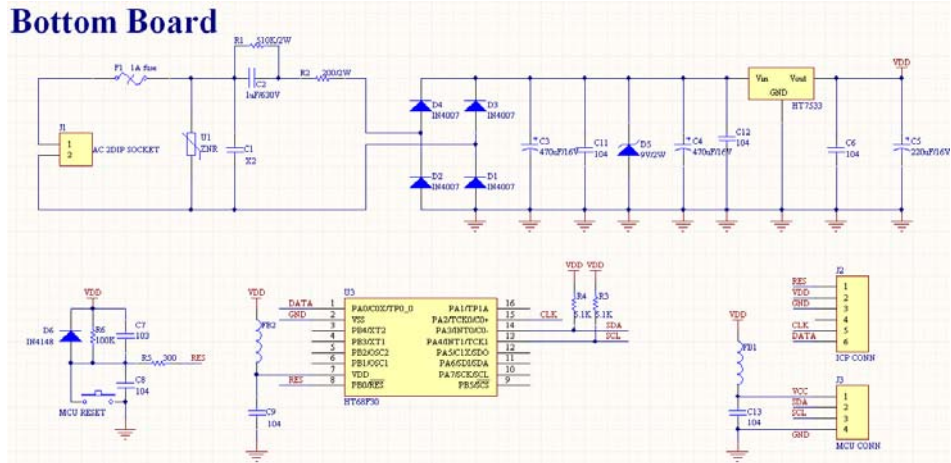


Figure 13 Bottom Board Application Circuit

Bottom Board: An AC-DC regulator circuit provides the 3.3V DC power supply for the HT68F30 & HT16C21, MCU -- HT68F30. The ICP interface J2 is for users to program code. The I<sup>2</sup>C communication interface is J3.

Note: for circuit debug, the capacitance C4 is not required.

## S/W Flowchart

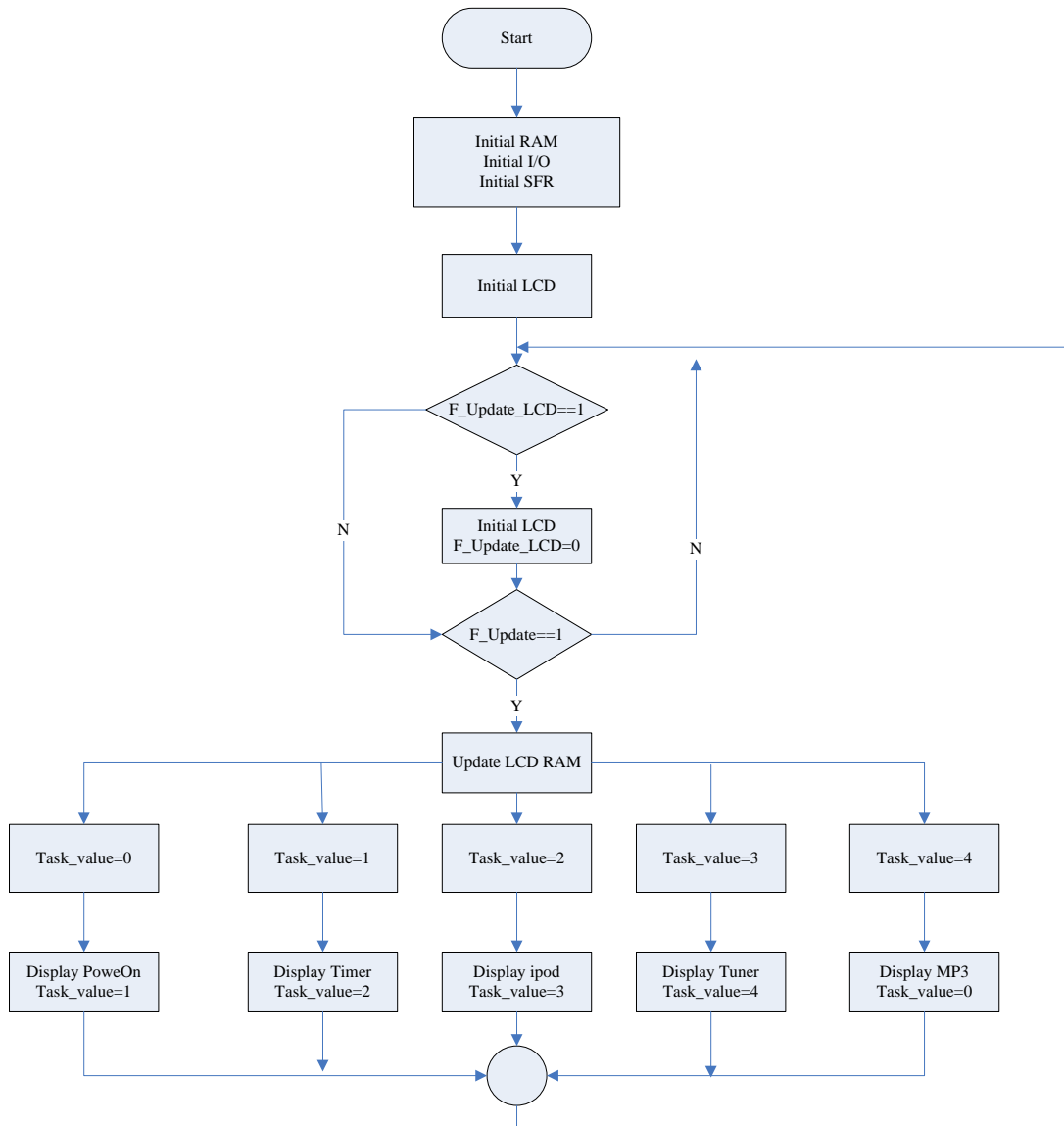


Figure 14 Main Flowchart Diagram

### Main Flowchart Diagram Description

After MCU power on, the program clears the RAM, initialises the I/O and the SFR. Then enable TM0 to be in the timing mode with a setup time of 4ms. Initialise the parameters used in the program and the HT16C21 through the I<sup>2</sup>C communication bus.

After initialisation, enter the main flow. Clear the watchdog, the program enters the display data process and the LCD RAM update routine. Determine if a time of 4ms has elapsed ? If yes, update the LCD RAM, execute the task according to the value of task\_value. If not, determine if 100ms has elapsed ? If the time has elapsed, initialise the LCD to improve the system ESD and EFT capability. If not, return to the main program.

## Display Steps Description

- Step0: initialisation after power on
  - After booting, the screen lights up for 3 seconds, flashes 3 times and enters the next stage.
  - Display 16C21for 3S.
- Step1: time display stage
  - Display the current time 12:36 for 2S, and then display 12:37 for 2S.
  - Display Alarm 1 Setting. After the Hour Setting flashes three times, the alarm can be set. The Hour ranges from 0 to 7. The Minute setting flashes three times, then the minutes can be set. The Minutes range from 0 to 24.
  - Display Alarm 2 Setting. After the Hour Setting flashes three times, the alarm can be set. The Hour ranges from 0 to 22. The Minute setting flashes three times, then the minutes can be set. The Minute ranges from 0 to 38.
- Step2: ipod mode
  - Display ipod, display play list 1 for 2s, and timing starts.
  - Display treble, display 15.4db for 2s, then increase 0.1 db every 0.5 second, at the same time ST is flashing. When it reaches 17.9db, keep displaying for 2s.
  - Switch to play list 2, the display flashes the normal time for 2s, and then displays the playing time.
  - Display bass, display 21.7db for 2s, then decrease 0.1 db every 0.5 second, at the same time ST is flashing. When it has reduced to 19.8db, keep displaying for 2s.
  - Exit ipod mode, the normal time remains displayed dynamically for 3s.
- Step3: Tuner-FM/AM
  - Tuner and AM are illuminated, display 987.6kHz for 2s, and then search the channels by increasing the frequency. The frequency increases by 0.1K every 0.1s up to 537.6kHz then stops, the tuner flashes once every 0.5s, keep this for 2s. At the same time it displays the normal time dynamically.
  - Search channels by reducing the frequency. The frequency decreases by 0.1K every 0.1s down to 993.1 KHz and then stops, tuner flashes every 0.5s, keep this for 2s.
  - Tuner and FM are illuminated, display 96.7MHz for 2s, and then search the channels by increasing the frequency. The frequency increases by 0.1M every 0.1s up to 84.6MHz and then stops, tuner flashes once every 0.5s, keep this for 2s. At the same time display the normal time dynamically.
  - Search channels by reducing the frequency. The frequency decreases by 0.1M every 0.1s down to 94.2MHz and then stops, tuner flashes every 0.5s, keep this for 2s.
  - Exit tuner mode, the normal time remains displayed dynamically for 2s.
- Step4: MP3 mode
  - Display MP3, display play list 3 for 2s, and timing starts.
  - Display treble, display 17.8 db for 2s, then increase by 0.1 db every 0.5 second, at the same time ST is flashing. When it reaches 19.0 db, keep displaying for 2s.
  - Switch to play list 4, display flashes the normal time for 2s, and then displays the playing time.
  - Display bass, display 19.8 db for 2s, then decrease 0.1 db every 0.5 second, at the same time ST is flashing. When it has reduced to 17.8db, keep displaying for 2s.
  - Exit the MP3 mode, the normal time remains displayed dynamically for 3s.
  - Return to the boot screen.

## Conclusions

This application uses the HT68F30 as the master MCU to control an Audio Panel LCD display and also introduced the HT16C21 features and related operations. The application gave some advice for programming so that users will have a better understanding of how to master HT16C21 applications.

## Accessory

Source Code File



HT16C21\_Demo\_Code.zip

PCB Figure File



HT16C21\_Demo\_PCB.zip