

HT32F125x Clock Monitor and Frequency Change

D/N : HA0283E

Overview

Introduction

This manual describes about the clock fail detection and the system frequency change of the HT32F125x microcontroller. The supported MCUs are HT32F125x series.

The clock monitor circuit can be used to detect the clock failures of the High Speed External Crystal Oscillator (HSE). If the HSE clock fails, it will be disabled and the High Speed Internal RC Oscillator (HSI) will automatically be switched as the system clock source. For more details refer to Section 2.1.

The system clock can be derived from the HSI, HSE and PLL clock. After reset, the HSI will be selected as the default system clock. When a clock source is used as the system clock, it cannot be disabled and must be ready before being used. Once the clock source switching occurs, the software must ensure that the process has been finished by polling the System Clock Switch bits in the Global Clock Control Register (GCCR).

The HSI clock has a fixed frequency of an internal 8 MHz oscillator. It can also be used as the PLL input clock. The HSI clock can be switched on or off by setting the HSIEN bit in the Global Clock Control Register (GCCR). When the HSI is powered up, it will not be released until the HSIRDY bit is set by hardware.

The HSE clock has a frequency of 4 to 16MHz crystal, producing a highly accurate clock source that is used as the system clock. It can also be used as the PLL input clock. The HSE clock can be switched on or off by setting the HSEEN bit in the Global Clock Control Register (GCCR). When the HSE is powered up, it will not be released until the HSERDY bit is set by hardware.

The PLL can provide 8 to 144MHz clock output which is the multiple of a fundamental reference frequency of 4 ~ 16MHz. While changing the clock source of the PLL, the new clock source must be ready before selection. The PLL can be switched on or off by setting the PLEN bit in the Global Clock Control Register (GCCR). If the PLL clock is stable, the PLLRDY bit is set by hardware.

HT32F125x Clock Control Bit Operation

HSE Clock Fail Detection

The HSE check function is enabled by setting the HSE Clock Monitor Enable bit (CKMEN) in the Global Clock Control Register (GCCR). The clock monitor should be enabled after an HSE oscillator start-up delay and disabled when this oscillator has stopped.

If an HSE failure is detected, this oscillator will be automatically disabled. An HSE clock stuck flag (CKSF) in the Global Clock Interrupt Register (GCIR) will be set. An interrupt will be generated if the clock fail interrupt enable bit (CKSIE) in the GCIR register has been set. This interrupt is connected to the exception vector of the CortexTM-M3 Non-Maskable Interrupt (NMI). In the NMI ISR, the clock stuck interrupt must be cleared by setting the CKSF bit in the GCIR register.

If the HSE is used as the system clock and HSE clock fails, the HSE will be turned off and the system clock will be switched to the HSI automatically by hardware.

If the HSE is used as PLL input clock and the PLL is used as the system clock, an HSE failure causes the system clock switching to HSI. Both HSE and PLL will be disabled by hardware, and then the HSI is also used as the PLL input clock.

System Frequency Change

The system clock source can be switched by setting the SW bits in the Global Clock Control Register (GCCR). If the system clock source is switched from one clock to another, the target clock source must be ready. The status bits in the Global Clock Status Register (GCSR) indicate which clock is ready. Once the clock source switching occurs, make sure that this process has been finished by polling SW bits in GCCR register. The SW bits must be read as the new clock source setting.

If the PLL is used as the system clock, the maximum system frequency is 72 MHz. The system frequency can be changed and the PLL configuration can be done without disabling PLL. The following steps show the procedure for changing the system frequency.

1. Select HSE or HSI as the system clock (SW [1:0] = 0x2 or 0x3). The HSE or HSI must be ready.
2. Poll SW bits until the value previously written becomes effective.
3. Set the AHBPRE bits to control the AHB prescaler. (AHBPRE [1:0] = 0x0)
4. Set the PLLCFGR register to reconfigure PLL output frequency. The PLL is enabled.
5. Poll PLLRDY bit until this flag is set in the GCSR register.
6. Set the AHBPRE bits.
7. Set the WAIT bits to control the Flash wait state.
8. Select PLL as the system clock (SW [1:0] = 0x0 or 0x1).
9. Poll SW bits until the value previously written becomes effective.

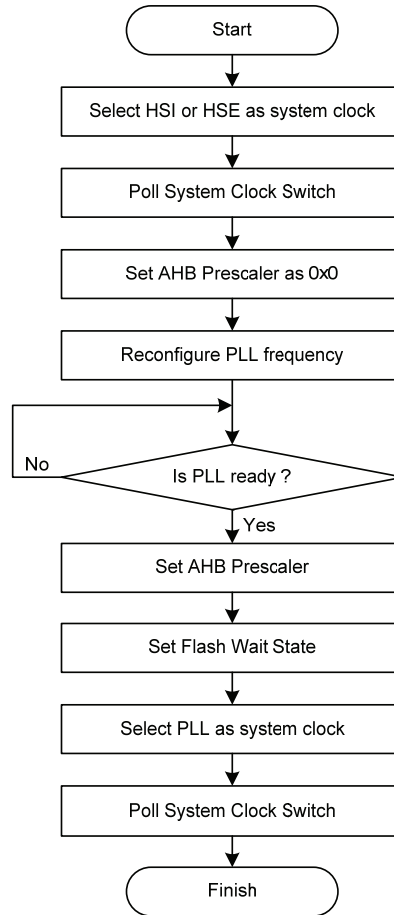


Fig.1 System Frequency Change Flowchart

Register Descriptions

The following table shows the CKCU registers and reset values.

Table 1 CKCU Register Map

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_8000			
GCFGR	0x000	Global clock configuration register	0x0000_0102
GCCR	0x004	Global clock control register	0x0000_0803
GCSR	0x008	Global clock status register	0x0000_0028
GCIR	0x00C	Global clock interrupt register	0x0000_0000
PLLCFGR	0x018	PLL configuration register	0x0000_0000
PLLCR	0x01C	PLL control register	0x0000_0000
AHBCFGR	0x020	AHB configuration register	0x0000_0000
AHBCCR	0x024	AHB clock control register	0x0000_0005
APBCFGR	0x028	APB configuration register	0x0000_0000
APBCCR0	0x02C	APB clock control register 0	0x0000_0000
APBCCR1	0x030	APB clock control register 1	0x0000_0000
CKST	0x034	Clock source status register	0x0100_0000
LPCR	0x300	Low power control register	0x0000_0000
MCUDBGCR	0x304	MCU debug control register	0x0000_0000

Global Clock Configuration Register – GCFGR

This register specifies the clock source for the PLL/USART/Watchdog Timer/CKOUT circuits.

Offset 0x000

Reset Value

	31	30	29	28	27	26	25	24
	LPMOD			Reserved				
Type/Reset	RO0	RO0	RO0					
	23	22	21	20	19	18	17	16
	Reserved		URPRE	Reserved				
Type/Reset			RW 0	RW 0				
	15	14	13	12	11	10	9	8
	Reserved							PLLSRC
Type/Reset								RW 1
	7	6	5	4	3	2	1	0
	Reserved				WDTSRC	CKOUTSRC		
Type/Reset					RW 0	RW 0	RW 1	RW 0

Bits	Field	Description
[31:29]	LPMOD	Lower Power Mode Status Set and reset by hardware. b000: Device is in run mode b001: Device is going to enter Sleep mode b010 :Device is going to enter Deep Sleep mode1 b011: Device is going to enter Deep Sleep mode2 b100: Device is going to enter Power Down mode Others: Reserved
[21:20]	URPRE	USART Clock Prescaler Selection Set and reset by software to control the USART clock prescaler value. b00:CK_USART = CK_UR b01: CK_USART = CK_UR / 2 Others: Reserved
[8]	PLLSRC	PLL Clock Source Selection Set and reset by software to control the PLL clock source. 0: External 4 ~ 16 MHz crystal oscillator clock is selected (HSE) 1: Internal 8 MHz RC oscillator clock is selected (HSI)
[3]	WDTSRC	Watchdog Timer Clock Source Selection Set and reset by software to control the Watchdog Timer clock source. 0: Internal LSI 32 kHz RC oscillator clock is selected 1: External LSE 32,768 Hz crystal oscillator clock is selected
[2:0]	CKOUTSRC	CKOUT Clock Source Selection Set and reset by software. 000: (CK_PLL / 16) is selected 001: (CK_AHB / 16) is selected 010: (CK_SYS / 16) is selected 011: (CK_HSE / 16) is selected 100: (CK_HSI / 16) is selected 101: CK_LSE is selected 110: CK_LSI is selected 111: Reserved

Global Clock Control Register – GCCR

This register specifies the clock enable bits.

Offset	0x004									
Reset	0x0000_0803									
		31	30	29	28	27	26	25	24	
Type/Reset		Reserved								
		23	22	21	20	19	18	17	16	
Type/Reset		Reserved						PSRCEN	CKMEN	
								RW 0	RW 0	
		15	14	13	12	11	10	9	8	
Type/Reset		Reserved				HSIEN	HSEEN	PLLEN	Reserved	
						RW 1	RW 0	RW 0		
		7	6	5	4	3	2	1	0	
Type/Reset		Reserved						SW		
								RW 1	RW 1	

Bits	Field	Description
[17]	PSRCEN	Power Saving Wakeup RC Clock Enable 0: No action 1: Use Internal 8 MHz HSI RC clock as the temporary system clock after waking up from either Deep-Sleep mode 1 or 2. Software should set PSRCEN before entering the power saving modes in order to reduce the waiting time after a wakeup. When the PSRCEN bit is set to 1, the HSI oscillator will be selected as the clock source after the system wakes up from the Deep-Sleep mode 1 or 2. Here, instruction execution can start quickly as the HSI clock is provided to the Cortex TM -M3. After the original system clock source has stabilized, which is the system clock, CK_SYS, before entering the Deep-Sleep mode 1 or 2, it will be then switched for use as the system clock.
[16]	CKMEN	HSE Clock Monitor Enable 0: Disable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor 1: Enable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor When the hardware detects that the HSE clock is stuck at a low or high state, the internal hardware will switch the system clock to be the internal high speed HSI RC clock. The way to recover the original system clock is by either an external reset, power on reset or clearing CKSF by software. Note: When the HSE clock monitor is enabled, the hardware will automatically enable the HSI internal RC oscillator regardless of the control bit, HSIEN, state.
[11]	HSIEN	Internal High Speed oscillator Enable Set and reset by software. This bit can not be reset if the HSI clock is used as the system clock. 0: Internal 8 MHz RC oscillator disabled 1: Internal 8 MHz RC oscillator enabled
[10]	HSEEN	External High Speed oscillator Enable Set and reset by software. This bit can not be reset if the HSE clock is used as the system clock or the PLL input clock. 0: External 4 ~ 16 MHz crystal oscillator is disabled 1: External 4 ~ 16 MHz crystal oscillator is enabled

Bits	Field	Description
[9]	PLLEN	<p>PLL Enable</p> <p>Set and reset by software. This bit cannot be reset if the PLL clock is used as the system clock.</p> <p>0: PLL is switched off</p> <p>1: PLL is switched on</p>
[1:0]	SW	<p>System Clock Switch</p> <p>Set and reset by software to select the CK_SYS source. Set by hardware to force the HSI (SW[1:0] = 0x03) to be used upon clock failure of the HSE oscillator if used directly or indirectly as the system clock (If the clock monitor is enabled). This field can be read back by software to indicate the currently used system clock source. Because system clock switching has some inherent latency, this field is set by software.</p> <p>0X: PLL output clock CK_PLL as system clock</p> <p>10: HSE clock CK_HSE as system clock</p> <p>11: HSI clock CK_HSI as system clock</p>

Global Clock Status Register – GCSR

This register indicates the clock ready status.

Offset	0x008
Reset Value	0x0000_0028
	<div style="display: flex; justify-content: space-between; border-bottom: 1px solid black; padding-bottom: 2px;"> 3130292827262524 </div> <div style="border: 1px solid black; height: 15px; width: 100%; text-align: center; margin-top: 2px;">Reserved</div>
Type/Reset	
	<div style="display: flex; justify-content: space-between; border-bottom: 1px solid black; padding-bottom: 2px;"> 2322212019181716 </div> <div style="border: 1px solid black; height: 15px; width: 100%; text-align: center; margin-top: 2px;">Reserved</div>
Type/Reset	
	<div style="display: flex; justify-content: space-between; border-bottom: 1px solid black; padding-bottom: 2px;"> 15141312111098 </div> <div style="border: 1px solid black; height: 15px; width: 100%; text-align: center; margin-top: 2px;">Reserved</div>
Type/Reset	
	<div style="display: flex; justify-content: space-between; border-bottom: 1px solid black; padding-bottom: 2px;"> 76543210 </div> <div style="display: flex; justify-content: space-between; border: 1px solid black; padding: 2px;"> <div style="width: 12.5%; text-align: center;">Reserved</div> <div style="width: 12.5%; text-align: center;">LSIRDY</div> <div style="width: 12.5%; text-align: center;">LSERDY</div> <div style="width: 12.5%; text-align: center;">HSIRDY</div> <div style="width: 12.5%; text-align: center;">HSERDY</div> <div style="width: 12.5%; text-align: center;">PLLRDY</div> <div style="width: 12.5%; text-align: center;">Reserved</div> </div>
Type/Reset	<div style="display: flex; justify-content: space-around; width: 100%;"> RO 1RO 0RO 1RO 0RO 0 </div>

Bits	Field	Description
[5]	LSIRDY	<p>LSI Internal Low Speed Oscillator Ready Flag</p> <p>Set by hardware to indicate if the LSI oscillator is stable and ready for use.</p> <p>0: LSI oscillator is not ready</p> <p>1: LSI oscillator is ready</p>
[4]	LSERDY	<p>LSE External Low Speed Oscillator Ready Flag</p> <p>Set by hardware to indicate if the LSE oscillator is stable and ready for use.</p> <p>0: LSE oscillator is not ready</p> <p>1: LSE oscillator is ready</p>
[3]	HSIRDY	<p>HSI High Speed Internal Oscillator Ready Flag</p> <p>Set by hardware to indicate if the HSI oscillator is stable and ready for use.</p> <p>0: HSI oscillator is not ready</p> <p>1: HSI oscillator is ready</p>

Bits	Field	Description
[2]	HSERDY	HSE High Speed External Clock Ready Flag Set by hardware to indicate if the HSE oscillator is stable and ready for use. 0: HSE oscillator is not ready 1: HSE oscillator is ready
[1]	PLLRDY	PLL Clock Ready Flag Set by hardware to indicate if the PLL output clock is stable and ready for use. 0: PLL is not ready 1: PLL is ready

Global Clock Interrupt Register – GCIR

This register specifies the interrupt enable and flag bits.

Offset	0x00C																								
Reset Value	0x0000_0000																								
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31	30	29	28	27	26	25	24																		
Reserved																									
Type/Reset																									
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; text-align: center;">23</td> <td style="width: 12.5%; text-align: center;">22</td> <td style="width: 12.5%; text-align: center;">21</td> <td style="width: 12.5%; text-align: center;">20</td> <td style="width: 12.5%; text-align: center;">19</td> <td style="width: 12.5%; text-align: center;">18</td> <td style="width: 12.5%; text-align: center;">17</td> <td style="width: 12.5%; text-align: center;">16</td> </tr> <tr> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">LSIRDYIE</td> <td style="text-align: center;">LSERDYIE</td> <td style="text-align: center;">HSIRDYIE</td> <td style="text-align: center;">HSERDYIE</td> <td style="text-align: center;">PLLRDYIE</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">CKSIE</td> </tr> <tr> <td style="text-align: center;">Type/Reset</td> <td style="text-align: center;">RW0</td> <td style="text-align: center;">RW0</td> <td style="text-align: center;">RW0</td> <td style="text-align: center;">RW0</td> <td style="text-align: center;">RW0</td> <td style="text-align: center;">Reserved</td> <td style="text-align: center;">RW0</td> </tr> </table>		23	22	21	20	19	18	17	16	Reserved	LSIRDYIE	LSERDYIE	HSIRDYIE	HSERDYIE	PLLRDYIE	Reserved	CKSIE	Type/Reset	RW0	RW0	RW0	RW0	RW0	Reserved	RW0
23	22	21	20	19	18	17	16																		
Reserved	LSIRDYIE	LSERDYIE	HSIRDYIE	HSERDYIE	PLLRDYIE	Reserved	CKSIE																		
Type/Reset	RW0	RW0	RW0	RW0	RW0	Reserved	RW0																		
Type/Reset																									
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%; text-align: center;">15</td> <td style="width: 12.5%; text-align: center;">14</td> <td style="width: 12.5%; text-align: center;">13</td> <td style="width: 12.5%; text-align: center;">12</td> <td style="width: 12.5%; text-align: center;">11</td> <td style="width: 12.5%; text-align: center;">10</td> <td style="width: 12.5%; text-align: center;">9</td> <td style="width: 12.5%; text-align: center;">8</td> </tr> <tr> <td colspan="8" style="text-align: center;">Reserved</td> </tr> </table>		15	14	13	12	11	10	9	8	Reserved															
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7	6	5	4	3	2	1	0																		
Reserved	LSIRDYF	LSERDYF	HSIRDYF	HSERDYF	PLLRDYF	Reserved	CKSF																		
Type/Reset	WC0	WC0	WC0	WC0	WC0	Reserved	WC0																		
Type/Reset																									

Bit	Field	Description
[22]	LSIRDYIE	LSI Ready Interrupt Enable LSI stabilization interrupt enable/disable control 0: Disable the LSI stabilization interrupt 1: Enable the LSI stabilization interrupt
[21]	LSERDYIE	LSE Ready Interrupt Enable LSE stabilization 0: Disable the LSE stabilization interrupt 1: Enable the LSE stabilization interrupt
[20]	HSIRDYIE	HSI Ready Interrupt Enable Set and reset by software to enable/disable the HSI stabilization interrupt 0: Disable the HSI stabilization interrupt 1: Enable the HSI stabilization interrupt
[19]	HSERDYIE	HSE Ready Interrupt Enable Set and reset by software to enable/disable the HSE stabilization interrupt 0: Disable the HSE stabilization interrupt 1: Enable the HSE stabilization interrupt

Bit	Field	Description
[18]	PLLRDYIE	PLL Ready Interrupt Enable Set and reset by software to enable/disable the PLL stabilization interrupt 0: Disable the PLL stabilization interrupt 1: Enable the PLL stabilization interrupt
[16]	CKSIE	Clock Stuck Interrupt Enable Set and reset by software to enable/disable the clock monitor interrupt 0: Disable the clock fail interrupt 1: Enable the clock fail interrupt
[6]	LSIRDYF	LSI Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the Internal 32 kHz RC oscillator clock is stable and the LSIRDYDIE bit is set. 0: No LSI stabilization clock ready interrupt is generated 1: LSI stabilization interrupt is generated
[5]	LSERDYF	LSE Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the External 32,768 Hz crystal oscillator clock is stable and the LSERDYDIE bit is set. 0: No LSE stabilization interrupt is generated 1: LSE stabilization interrupt is generated
[4]	HSIRDYF	HSI Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the Internal 8 MHz RC oscillator clock is stable and the HSIRDYDIE bit is set. 0: No HSI stabilization interrupt is generated 1: HSI stabilization interrupt is generated
[3]	HSERDYF	HSE Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the External 4 ~ 16 MHz crystal oscillator clock is stable and the HSERDYDIE bit is set. 0: No HSE stabilization interrupt is generated 1: HSE stabilization interrupt is generated
[2]	PLLRDYF	PLL Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the PLL is stable and the PLLRDYDIE bit is set. 0: No PLL stabilization interrupt is generated 1: PLL stabilization interrupt is generated
[0]	CKSF	HSE Clock Stuck Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the HSE clock is stuck and the CKSIE bit is set. 0: Clock operating normally 1: HSE clock stuck

PLL Configuration Register – PLLCFGR

This register specifies the PLL configuration.

Offset 0x018
Reset Value 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				PFBD [5:1]			
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PFBD[0]	POTD		Reserved				
Type/Reset	RW 0	RW 0	RW 0					
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bit	Field	Description
[28:23]	PFBD	PLL VCO Output Clock Feedback Divider (B5 ~ B0) Feedback Divider divides the output clock from the PLL VCO.
[22:21]	POTD	PLL Output Clock Divider (S1 ~ S0)

PLL Control Register – PLLCR

This register specifies the PLL Bypass mode.

Offset 0x01C
Reset Value 0x0000_0000

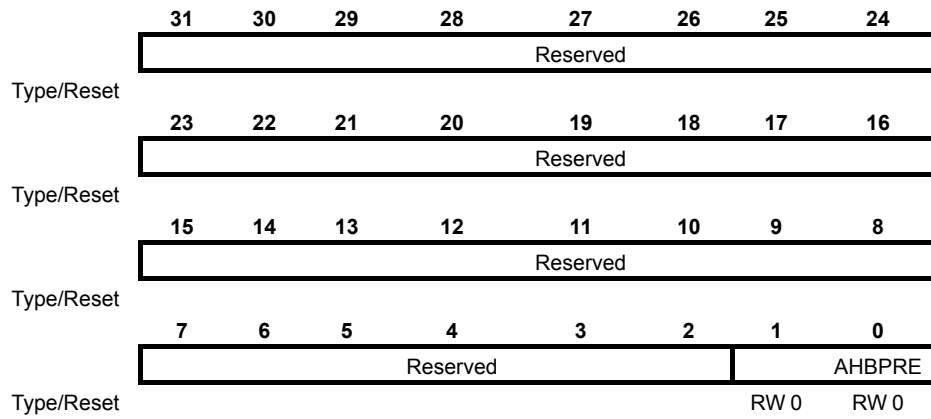
	31	30	29	28	27	26	25	24
	PLLBPS	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bit	Field	Description
[31]	PLLBPS	PLL Bypass Mode Enable 0: Disable the PLL Bypass mode 1: Enable the PLL Bypass mode in which the PLL output clock PLLOUT is equal to the CKIN clock

AHB Configuration Register – AHBCFGR

This register specifies the system clock frequency.

Offset 0x020
 Reset Value 0x0000_0000



Bit	Field	Description
[1:0]	AHBPRES	AHB Pre-Scalar Set and reset by software to control the AHB clock division ratio. 00: CK_AHB = CK_SYS 01: CK_AHB = CK_SYS / 2 10: CK_AHB = CK_SYS / 4 11: CK_AHB = CK_SYS / 8

AHB Clock Control Register – AHBCCR

This register specifies the AHB clock enable bits.

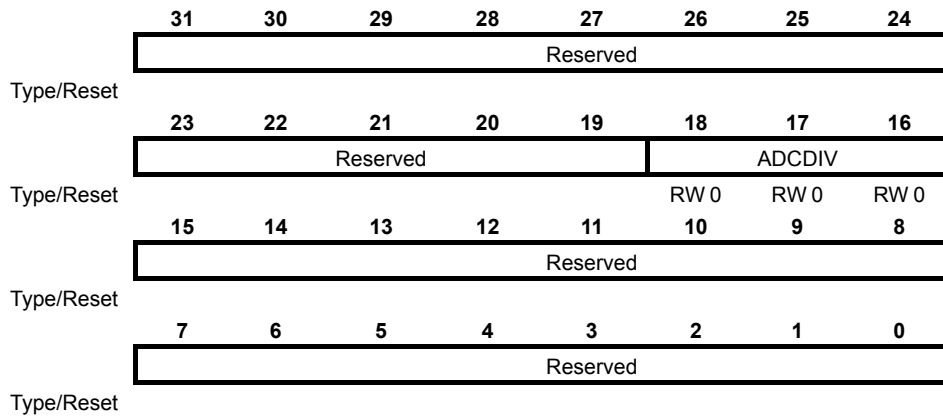
Offset	0x024									
Reset Value	0x0000_0005									
		31	30	29	28	27	26	25	24	
Type/Reset		Reserved								
		23	22	21	20	19	18	17	16	
Type/Reset		Reserved								
		15	14	13	12	11	10	9	8	
Type/Reset		Reserved								
		7	6	5	4	3	2	1	0	
Type/Reset		Reserved					SRAMEN	Reserved	FMCEN	
							RW 1		RW 1	

Bit	Field	Description
[2]	SRAMEN	SRAM Clock Enable Set and reset by software. Clear the SRAMEN bit to 0 to reduce power consumption if the SRAM is unused in the Sleep mode. 0: SRAM clock is disabled in Sleep mode 1: SRAM clock is enabled in Sleep mode
[0]	FMCEN	Flash Memory Controller Clock Enable Set and reset by software. Clear the FMCEN bit to 0 to reduce power consumption if the Flash Memory is unused in the Sleep mode. 0: FMC clock is disabled in Sleep mode 1: FMC clock is enabled in Sleep mode

APB Configuration Register – APBCFGR

This register specifies the ADC clock frequency.

Offset 0x028
Reset Value 0x0000_0000



Bit	Field	Description
[18:16]	ADCDIV	ADC Clock Frequency Division Select Set and reset by software to control the ADC clock division ratio. 000: CK_ADC = CK_AHB 001: CK_ADC = (CK_AHB / 2) 010: CK_ADC = (CK_AHB / 4) 011: CK_ADC = (CK_AHB / 8) 100: CK_ADC = (CK_AHB / 16) 101: CK_ADC = (CK_AHB / 32) 110: CK_ADC = (CK_AHB / 64) 111: CK_ADC = (CK_AHB / 6)

Clock Source Status Register – CKST

This register specifies the clock source status.

Offset 0x034
Reset Value 0x0100_0000

	31	30	29	28	27	26	25	24
	Reserved					HSIST		
Type/Reset						RO0	RO0	RO1
	23	22	21	20	19	18	17	16
	Reserved						HSEST	
Type/Reset							RO0	RO0
	15	14	13	12	11	10	9	8
	Reserved							PLLST
Type/Reset								RO0
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bit	Field	Description
[26:24]	HSIST	High Speed Internal Clock Occupation Status (CK_HSI) xx1: HSI used by System Clock (CK_SYS) (SW = 0x03) x1x: HSI used by PLL 1xx: HSI used by Clock Monitor
[17:16]	HSEST	High Speed External Clock Occupation Status (CK_HSE) x1: HSE is used by System Clock (CK_SYS) (SW = 0x02) 1x: HSE is used by PLL
[8]	PLLST	PLL Clock Occupation Status 0: PLL is not used by System Clock (CK_SYS) 1: PLL is used by System Clock (CK_SYS)

Low Power Control Register – LPCR

This register specifies the low power control bit.

Offset	0x300																
Reset Value	0x0000_0000																
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7	6	5	4	3	2	1	0										
Reserved							BKISO										
Type/Reset	R/W 0																

Bit	Field	Description
[0]	BKISO	Backup Domain Isolation Control Set and reset by software. Refer to the Power Control Unit chapter for more information. 0: Backup domain is isolated from other power domains 1: Backup domain is accessible by other power domains

MCU Debug Control Register – MCUDBGCR

This register specifies the MCU debug control.

Offset	0x304
Reset Value	0x0000_0000
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 3130292827262524 </div> <div style="border: 1px solid black; height: 15px; width: 100%; text-align: center; margin-top: 5px;">Reserved</div>	
Type/Reset	
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 2322212019181716 </div> <div style="border: 1px solid black; height: 15px; width: 100%; text-align: center; margin-top: 5px;">Reserved</div>	
Type/Reset	
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 15141312111098 </div> <div style="display: flex; justify-content: space-between; padding: 0 10px; border: 1px solid black; margin-top: 5px;"> ReservedDBDSSLP2ReservedDBSPIReservedDBUSART </div>	
Type/Reset	<div style="display: flex; justify-content: space-between; padding: 0 10px;"> R/W 0R/W 0R/W 0 </div>
<div style="display: flex; justify-content: space-between; padding: 0 10px;"> 76543210 </div> <div style="display: flex; justify-content: space-between; padding: 0 10px; border: 1px solid black; margin-top: 5px;"> DBGPTM1DBGPTM0ReservedDBWDTDBPDDBDSSLP1DBSLP </div>	
Type/Reset	<div style="display: flex; justify-content: space-between; padding: 0 10px;"> R/W 0R/W 0R/W 0R/W 0R/W 0R/W 0 </div>

Bit	Field	Description
[14]	DBDSSLP2	Debug Deep-Sleep mode 2 Set and reset by software. 0: LDO = Off, DMOS = On, FCLK = Off and HCLK = Off in Deep-Sleep2 1: LDO = On, FCLK = On and HCLK = On in Deep-Sleep mode 2
[10]	DBSPI	SPI Debug Mode Enable Set and reset by software. This bit is used to control whether the SPI timeout mode is stopped or not when the core is halted. 0: Same behavior as normal mode 1: SPI FIFO timeout is stopped
[8]	DBUSART	USART Debug Mode Enable Set and reset by software. This bit is used to control whether the USART timeout mode is stopped or not when the core is halted. 0: Same behavior as normal mode 1: USART RX FIFO timeout is stopped
[7]	DBGPTM1	GPTM1 Debug Mode Enable Set and reset by software. This bit is used to control whether the GPTM1 counter is stopped or not when the core is halted. 0: GPTM1 counter keeps counting even if the core is halted 1: GPTM1 counter is stopped when the core is halted
[6]	DBGPTM0	GPTM0 Debug Mode Enable Set and reset by software. This bit is used to control whether the GPTM0 counter is stopped or not when the core is halted. 0: GPTM0 counter keeps counting even if the core is halted 1: GPTM0 counter is stopped when the core is halted
[3]	DBWDT	Watchdog Timer Debug Mode Enable Set and reset by software. This bit is used to control whether the Watchdog Timer Counter is stopped or not when the core is halted. 0: Watchdog Timer counter keeps counting even if the core is halted 1: Watchdog Timer counter is stopped when the core is halted
[2]	DBPD	Debug Power-Down Mode Set and reset by software. 0: LDO = Off, FCLK = Off and HCLK = Off in Power-Down mode 1: LDO = On, FCLK = On and HCLK = On in Power-Down mode

Bit	Field	Description
[1]	DBDSLP1	Debug Deep-Sleep mode 1 Set and reset by software. 0: LDO = Low power mode, FCLK = Off and HCLK = Off in Deep-Sleep1 1: LDO = On, FCLK = On and HCLK = On in Deep-Sleep mode 1
[0]	DBSLP	Debug Sleep Mode Set and reset by software. 0: LDO = On, FCLK = On and HCLK = Off in Sleep mode 1: LDO = On, FCLK = On and HCLK = On in Sleep mode