HT32F125x Flash Programming

D/N: HA0282E

Overview

Introduction

This manual describes the HT32F125x series microcontroller flash programming methods. The supported MCUs are **HT32F1253**, **HT32F1252**, **HT32F1251** and **HT32F1251B**.

The HT32F125x series devices embedded Flash can be programmed in several ways such as using In-System Programming (ISP), In-Application Programming (IAP) or In-Circuit Programming (ICP).

While the application is running, IAP is an important method to re-program the Flash. This can be used for firmware upgrades using specific communication types such as USB, USART, etc. IAP applications will be programmed in Flash using an ICP method.

ISP is similar to IAP for updating the Flash memory except that it is located in the bootloader which is programmed by Holtek using the USART as the only communication protocol.

The in-circuit programming (ICP) method is used to download the whole Flash memory data. Both the Joint Test Action Group (JTAG) and Serial Wire Debug (SWD) interfaces can be used to load the program data into the microcontroller. The HT32F125x supports only the SWD interface.

The Flash interface performs instruction access and data access via the I-Code and D-Code bus of the Cortex-M3 core respectively. A pre-fetch buffer is used to reduce instruction gaps. The Flash operations include Program, Page Erase and Mass Erase and also Read/Write protection functions.

Features

- Up to 32 KB of on-chip Flash memory
  - HT32F1253: 31 KB + 1 KB - instruction/data + option bytes
  - HT32F1252: 16 KB + 1 KB - instruction/data + option bytes
  - HT32F1251(B): 8 KB + 1 KB - instruction/data + option bytes
- 1 KB Page size
- Wide read interface with pre-fetch buffer
- Flash program / page erase / mass erase capability
- Interrupt capability
- Read protection
- Page erase / program protection

Flash Memory Architecture

The Flash memory consists of a main block of up to 32 KB and an information block. The main block contains up to 32 pages of 1 KB each. Refer to Table 1, Table 2 and Table 3 for details.

The Flash memory is implemented using 32-bit words for both instruction and data storage. The Flash memory is located at specific addresses in the HT32F125x memory map.

The main block write operation is controlled by the Flash Memory Controller, otherwise known as the FMC. The FMC manages the program and erase procedures.

The information block is reserved for the bootloader which is then used as an ISP to re-program the main block using the USART. The device can be booted in the Bootloader boot mode if both BOOT0 & BOOT1 are pulled low.

The Flash memory can also be protected against any unexpected read/write/page erase operations. For more details refer to Section 2.4.

During write or erase operations, read operations cannot be executed.

The High Speed Internal RC Oscillator, his, must be enabled before any write/erase operations are executed.

Table 1 HT32F1253 Flash Memory Architecture

Block	Name	Address	Page Protection Bit	Size
Main Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [1]	1KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [2]	1KB
	: :	: :	: :	: :
	Page 30	0x0000_7800 ~ 0x0000_7BFF	OB_PP [30]	1KB
	Option Byte	0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1KB
Option Byte	Boot Loader	0x1F00_0000 ~ 0x1FF0_07FF	NA	2KB

Table 2 HT32F1252 Flash Memory Architecture

Block	Name	Address	Page Protection Bit	Size
Main Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [1]	1KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [2]	1KB
	: :	: :	: :	: :
	Page 15	0x0000_3C00 ~ 0x0000_3FFF	OB_PP [15]	1KB
	Option Byte	0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1KB
Option Byte	Boot Loader	0x1F00_0000 ~ 0x1FF0_07FF	NA	2KB

Table 3 HT32F1251(B) Flash Memory Architecture

Block	Name	Address	Page Protection Bit	Size
Main Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [1]	1KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [2]	1KB
	: :	: :	: :	: :
	Page 7	0x0000_1C00 ~ 0x0000_1FFF	OB_PP [7]	1KB
	Option Byte	0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1KB
Information Block	Boot Loader	0x1F00_0000 ~ 0x1FF0_07FF	NA	2KB

HT32F125x Embedded Flash Operations

Read Operation

The embedded Flash memory is just like any other common type of memory in that it can be addressed directly. The access interface reads from the Flash memory and stores the instruction/data in the pre-fetch buffer. The pre-fetch buffer can be disabled if the enable bit, PFBE, in the Flash pre-fetch control register is reset. By default, the pre-fetch buffer will be on.

Program / Erase Operation

The Flash Memory Controller (FMC) provides the Flash memory program and erase functions.

Flash Programming

The FMC provides a 32-bit word programming function to write to the Flash memory. The following steps show the sequence.

1. Check the OPCR register to confirm that no Flash memory operation is ongoing (OPM [3:0] equal to 0xE, or 0x6). Otherwise wait until the previous operation has finished.
2. Write the word address into the TADR register.
3. Write the word data into the WRDR register.
4. Write the word program command into the OCMR register (CMD [3:0] = 0x4).
5. Send the word program command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
6. Wait until all operations are finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
7. Read and verify the Flash memory if required using a DCODE access.

Note: that an erase operation must be performed between two successive Flash programming operations at the same address. When an attempt is made to write to protected pages, a Flash operation error interrupt will be triggered by setting the OREIEN bit in the OIER register. Check the PPEF bit in the OISR register to detect this condition in the interrupt handler.

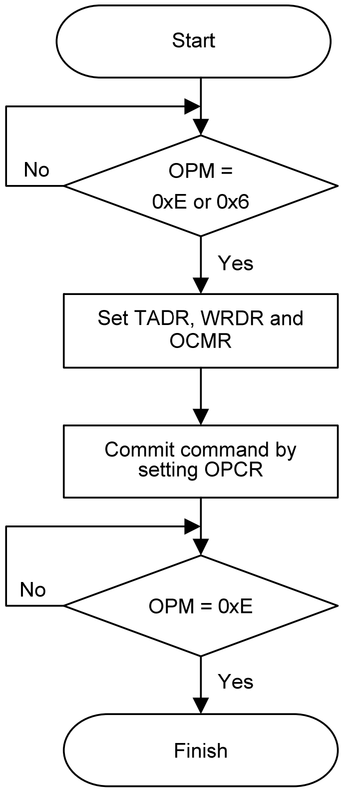

Figure 1 Flash Word Programming Flowchart

Page Erase

The FMC provides a page erase function which is used to erase the contents of a specific Flash page. Each page can be erased independently. The following steps show the page erase sequence.

1. Check the OPCR register to confirm that no Flash memory operation is ongoing (OPM [3:0] equal to 0xE or 0x6). Otherwise wait until the previous operation has finished.
2. Write the page address into the TADR register
3. Write the page erase command into the OCMR register (CMD [3:0] = 0x8).
4. Send the page erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
5. Wait until all the operations are finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
6. Read and verify the page if required using a DCODE access.

The correct address of the targeted page must be confirmed. The software may run out of control if the targeted erase page is being used for code or data fetching. Note that, the page erase operation will skip over the write protected pages. A Flash operation error interrupt will be triggered by setting the OREIEN bit in the OIER register. Check the PPEF bit in the OISR register to detect this condition in the interrupt handler.

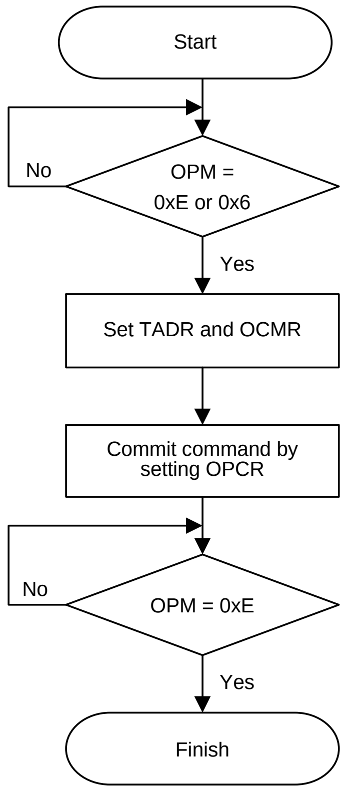

Figure 2 Flash Page Erase Flowchart

Mass Erase

The FMC provides a complete erase function which is used to erase all pages in the main block.

The following steps show the mass erase sequence.

1. Check the OPCR register to confirm that no Flash memory operation is ongoing (OPM [3:0] equal to 0xE or 0x6). Otherwise wait until the previous operation has finished.
2. Write the mass erase command into the OCMR register (CMD [3:0] = 0xA).
3. Send the mass erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
4. Wait until all operations are finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
5. Read and verify the Flash memory if required using a DCODE access.

When the mass erase operation has finished, the main block will be erased to 0xFFFF_FFFF. The mass erase command can be used by the program that runs in the SRAM or by the debugging tool.

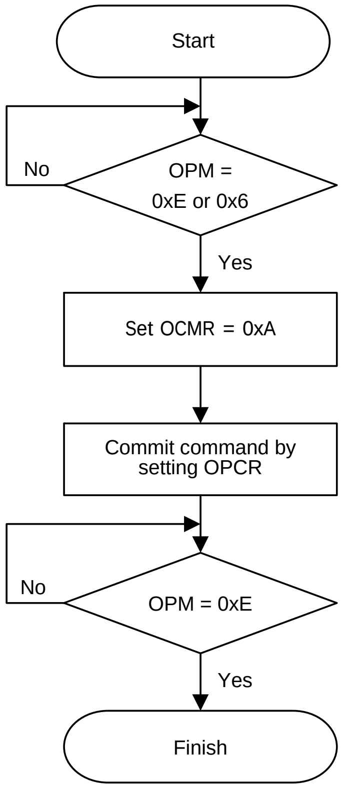

Figure 3 Flash Mass Erase Flowchart

Option Byte Block

The option byte block can be treated as an independent Flash memory whose base address is 0x1FF0_0000. The option bytes consist of 6 words that are used for Flash read/write protection functions.

After a reset, the option bytes will be reloaded and their contents will be stored into the registers. If the checksum of the option byte is incorrect, the checksum error (OBEF) will be generated in the OISR register.

Table 4 Option Byte Organisation

Option Byte	Offset	Description	Reset Value
Option Byte Base Address = 0x1FF0_0000			
OB_PP	0x000 0x004 0x008 0x00C	OB_PP [n]：Flash Memory Page Erase/Program Protection (n = 0 ~ 30 for page 0 ~ page 30) 0: Flash Memory Page n Erase/Program Protection is enabled 1: Flash Memory Page n Erase/Program Protection is disabled OB_PP [127:31] is reserved for future usage.	0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF
OB_CP	0x010	OB_CP [0]: Flash Security Protection 0: Flash Security protection is enabled 1: Flash Security protection is disabled OB_CP [1]: Option Byte Protection 0: Option Byte protection is enabled 1: Option Byte protection is disabled OB_CP [31:2]: Reserved	0xFFFF_FFFF
OB_CK	0x020	OB_CK [31:0]: Flash Option Byte Checksum OB_CK should be set as the sum of the 5 words Option Bytes content, of which the address offset is ranged form 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the content of the OB_PP or OB_CP register is not equal to 0xFFFF_FFFF.	0xFFFF_FFFF

Flash Protection

The main block of the Flash memory can be protected to prevent illegal access from untrusted code. The pages of the main block can also be protected independently to prevent any unexpected write operations.

- Security Protection
  This function is useful to provide protection from illegal users. The security protection is activated by setting the option byte OB_CP [0]. Once the protection has been enabled, the Flash DCODE access, program and page erase operations will not be allowed in the debug mode. Page 0 and the Option Byte block are also write-protected automatically. Mass erase operations can be performed to disable the security protection.
  - To enable the security protection, the procedure below should be followed.
    1. Program the OB_CP [0] as 0.
    2. Program the OB_CK as the sum of the 5 words option byte that is addressed from 0x0 to 0x13.
    3. Generate a system reset to activate the new OB_CP setting.
  - To disable the security protection, the procedure below should be followed.
    1. Perform a mass erase. At this point note that the security protection is still enabled.
    2. Generate a power-on reset to activate the new OB_CP setting.
- Write Protection
  Write protection can be individually enabled by setting OB_PP for each page of the main block. If a page erase or program operation is performed on a protected page, the PPEF bit in the OISR register will be set. If the OREIEN bit in the OIER register is also set, a Flash operation error interrupt will be triggered by the FMC.
  If a page erase operation is performed on an option byte block, all write protection functions will be disabled. The write protection of the option byte region is activated by setting OB_CP [1] to 0. If the option byte block has been protected, the only way to disable the write protection is to execute a mass erase operation.
  - To enable the write protection, the procedure below should be followed.
    1. Program the OB_PP [30:0] (for HT32F1253) as 0 to enable protection of the corresponding page. (program OB_PP[15:0] for HT32F1252, OB_PP[7:0] for HT32F1251(B))
       Program the OB_CP [1] as 0 to enable protection of the option byte block.
    2. Program the OB_CK as the sum of the 5 words option byte addressed from 0x0 to 0x13.
    3. Generate a system reset to activate the new OB_PP/OB_CP setting.
  - To disable the main block pages write protection, the procedure below should be followed.
    1. Erase the option byte block. The option byte should be unprotected.
    2. Generate a system reset to activate the new OB_PP setting.
  - To disable the write protection of option byte block, the procedure below should be followed.
    1. Perform a mass erase.
    2. Generate a system reset to activate the new OB_CP setting.

Register Descriptions

The following table shows the FMC registers and reset values.

Table 5 FMC Register Map

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt Status Register	0x0001_0000
PPSR	0x020 0x024 0x028 0x02C	Flash Page Erase/Program Protection Status Register	0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX
CPSR	0x030	Flash Security Protection Status Register	0xXXXX_XXXX
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X
CFCR	0x200	Flash Cache and Pre-fetch Control Register	0x0000_0051
SBVT0	0x300	SRAM Booting Vector 0 (Stack Pointer)	0x2000_XX00
SBVT1	0x304	SRAM Booting Vector 1 (Program Counter)	0x2000_0101
SBVT2	0x308	SRAM Booting Vector 2 (NMI Handler)	0x0000_0000
SBVT3	0x30C	SRAM Booting Vector 3 (Hard Fault Handler)	0x0000_0000
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000

"X" means various reset values which depend on the Device, Flash value, option byte value or power on reset setting.

Flash Target Address Register -- TADR

This register specifies the target address of the page erase and word programming operations.

Offset : 0x000
Reset value : 0x0000_0000

	31	30	29	28	27	26	25	24
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	TADB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0

Bits	Field	Descriptions
[31:0]	TADB	Flash Target Address Bits For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32 bits, TADR shall be set as word-aligned (4 bytes). TADB [1:0] will be ignored during programming operations. For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1KB, TADB [9:0] will be ignored in order to limit the target address to 1 kbyte-aligned. For 32KB main Flash addressing, TADB [31:16] should be zero (TADB [31:15] should be zero for 16KB, TADB [31:14] should be zero for 8 KB). The Option Byte which has a 1KB capacity ranges from 0x1FF0_0000 to 0x1FF0_03FF. This field is used to specify the Flash Memory address which must be within the range from 0x0000_0000 to 0x1FFF_FFFF. Otherwise, an Invalid Target Address interrupt will be generated if the corresponding interrupt enable bit is set.

Flash Write Data Register -- WRDR

This register stores the data to be written into the TADR register for programming operations.

Offset : 0x004
Reset value : 0x0000_0000

	31	30	29	28	27	26	25	24
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	23	22	21	20	19	18	17	16
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	15	14	13	12	11	10	9	8
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
	7	6	5	4	3	2	1	0
	WRDB							
Type/Reset	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0

Bits	Field	Descriptions
[31:0]	WRDB	Flash Write Data Bits The data value for programming operation.

Flash Operation Command Register -- OCMR

This register is used to specify the Flash operation commands that include read, read ID, word program, page erase and mass erase.

Offset : 0x00C
Reset value : 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved				CMD			
Type/Reset					RW0	RW0	RW0	RW0

Bits	Field	Descriptions
[3:0]	CMD	Flash Operation Command The following table shows the definitions of the operation command bits CMD [3:0] which determine the Flash Memory operation. If an invalid command is set and the IOCMIEN bit is equal to 1, an Invalid Operation Command interrupt will occur.

CMD [3:0]	Description
0x0	Idle - default
0x4	Word program
0x8	Page erase
0xA	Mass erase
Others	Reserved

Flash Operation Control Register -- OPCR

This register is used to control the command commitment and to check the status of the FMC operations.

Offset : 0x010
Reset value : 0x0000_000C

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved			OPM				Reserved
Type/Reset				RW0	RW0	RW0	RW0	

Bits	Field	Descriptions
[4:1]	OPM	Operation Mode The following table shows the FMC operation modes. The user can commit the command which is set by the OCMR register for the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR and OCMR registers should be prepared before setting this register. After all the operations have finished, the OPM field will be set as 0xE or 0xF by the FMC hardware. The Idle mode can be set when all the operations have finished for power saving purposes. Note that the operation status should be checked before the next operation is executed on the FMC. The contents of the TADR, WRDR, OCMR and OPCR registers should not be changed until the previous operation has finished.

OPM [3:0]	Description
0x6	Idle - default
0xA	Commit command to the main Flash
0xE	All operations finished on the main Flash
Others	Reserved

Flash Operation Interrupt Enable Register -- OIER

This register is used to enable or disable the FMC interrupt function. The FMC generates interrupts to the controller when the corresponding interrupt enable bits are set.

Offset : 0x014
Reset value : 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved			OREIEN	IOCMIEN	OBEIEN	ITADIEN	ORFIEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Operation Error interrupt is disabled 1: Operation Error interrupt is enabled
[3]	IOCMIEN	Invalid Operation Command Interrupt Enable 0: Invalid Operation Command interrupt is disabled 1: Invalid Operation Command interrupt is enabled
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Option Byte Check Sum Error interrupt is disabled 1: Option Byte Check Sum Error interrupt is enabled
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Invalid Target Address interrupt is disabled 1: Invalid Target Address interrupt is enabled
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Operation Finish interrupt is disabled 1: Operation Finish interrupt is enabled

Flash Operation Interrupt and Status Register -- OISR

This register indicates the FMC interrupt status that reports if a Flash operation has finished, otherwise an error occurs. The status bits are available when the corresponding interrupt enable bits in the OIER register are set.

Offset : 0x018

Reset value : 0x0001_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								

	23	22	21	20	19	18	17	16
	Reserved						PPEF	RORFF
Type/Reset							RO 0	RO 1

	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved			OREF	IOCMF	OBEF	ITADF	ORFF
Type/Reset				WC0	WC0	WC0	WC0	WC0

Bits	Field	Descriptions
[17]	PPEF	Page Erase/Program Protected Error Flag 0: Page Erase/Program Protected Error does not occur 1: Operation error occurs due to an invalid Page erase/program operation being applied to a protected page This bit is reset by hardware once a new flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last flash operation command has not yet finished 1: The last flash operation command has finished The RORFF bit is directly connected to the Flash memory for debugging purpose.
[4]	OREF	Operation Error Flag 0: No flash operation error has occurred 1: The last flash operation has failed This bit will be set when any flash operation errors such as an invalid command, program error and erase error, etc., occurs. The ORE interrupt occurs if the OREIEN bit in the OIER register is set. Reset this bit by writing a 1
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid flash operation command has been set 1: An invalid flash operation command has been written to the OCMR register. The IOCM interrupt will occur if the IOCMIEN bit in the OIER register is set. Reset this bit by writing a 1.
[2]	OBEF	Option Byte Checksum Error Flag 0: Option byte Checksum is correct 1: Option byte Checksum is incorrect The OBE interrupt will occur if the OBEIEN bit in the OIER register is set. Reset this bit by writing a 1.

Bits	Field	Descriptions
[1]	ITADF	Invalid Target Address Flag 0: The target address TADR is valid 1: The target address TADR is invalid The data in the TADR field must have a range from 0x0000_0000 to 0x1FFF_FFFF. An ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. Reset this bit by writing a 1.
[0]	ORFF	Operation Finished Flag 0: Flash operation unfinished. 1: Last flash operation command has finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. Reset this bit by writing a 1.

Flash Page Erase/Program Protection Status Register -- PPSR

This register indicates the page protection status of the Flash Memory.

Offset : 0x020 ~ 0x02C
Reset value : 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[127:0]	PPSBn	Page n Erase/Program Protection Status Bits (n = 0 ~ 127) PPSB[n] = OB_PP[n] 0: The corresponding page n is protected 1: The corresponding page n is not protected The content of this register is not dynamically updated and will only be reloaded by the option byte loader which is activated when any kind of reset occurs. The erase or program function of the specific pages is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of the bits PPSR [127:0] is determined by the option byte, OB_PP [127:0]. The total number of flash memory pages for the HT32F125x series will be different because of the different device specifications. Therefore, only the OB_PP [n:0] and PPSR [n:0] bits are valid (where n = chip flash page number - 1). The other bits of the OB_PP and PPSR registers are reserved for future usage.

Flash Security Protection Status Register -- CPSR

This register indicates the Flash Memory Security protection status. The content of this register is not dynamically updated and will only be reloaded by the option byte loader which is activated when any kind of reset occurs.

Offset : 0x030
Reset value : 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						OBPSB	CPSB
Type/Reset							RO X	RO X

Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase/Program Protection Status Bit 0: The Option Bytes page is protected. 1: The Option Bytes page is not protected. The reset value of the OPBSB bit is determined by the OB_CP [1] bit in the option byte.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Memory Security protection is enabled 1: Flash Memory Security protection is not enabled The reset value of the CPSB bit is determined by the OB_CP [0] bit in the option byte.

Flash Vector Mapping Control Register -- VMCR

This register is used to control the vector mapping. The reset value of the VMCR register is determined by the status of the external boot pins, BOOT0 and BOOT1 during the power on reset period.

Offset : 0x100
Reset value : 0x0000_000X

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved						VMCB	
Type/Reset							RW X	RW X

Bits	Field	Descriptions
[1:0]	VMCB	Vector Mapping Control Bit The VMCB bits are used to control the mapping source of the first 4-word vectors addressed from 0x0 to 0xC. The following table shows the vector mapping setup.

BOOT1	BOOT0	VMCB [1:0]	Descriptions
Low	Low	00	Boot Loader mode The vector mapping source is the boot loader area.
Low	High	01	SRAM booting mode The vector mapping source is SBVT0~ SBVT 3.
High	Low	10	Main Flash mode The vector mapping source is the main Flash Memory area.
High	High	11	

The reset value of the VMCB register is determined by the pin status of the external boot pins, BOOT1 and BOOT0, during a power on reset and a system reset. However, when the application program is executed, the vector mapping settings can be temporarily changed by configuring the VMCB bits to correctly access the first 4-word vectors in the flash memory, especially when the CPU is booted from the Boot Loader or the SRAM region.

Flash Pre-fetch Control Register -- CFCR

This register is used to control the FMC pre-fetch module.

Offset : 0x200
Reset value : 0x0000_0051

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved	IPSE	Reserved	PFBE	Reserved	WAIT		
Type/Reset		RW 1		RW 1		RW 0	RW 0	RW 1

Bits	Field	Descriptions
[6]	IPSE	Flash Idle Power Saving Enable Bit 0: Flash Idle Power Saving is disabled 1: Flash Idle Power Saving is enabled
[4]	PFBE	Pre-fetch Buffer Enable Bit 0: Pre-fetch buffer is disabled. Instructions/Data are provided directly by the Flash memory. 1: Pre-fetch buffer is enabled
[2:0]	WAIT	Flash Wait State Setting These bits are used to set the HCLK wait clock count during a non-sequential Flash access. The actual value of the wait clocks is given by (WAIT [2:0] - 1). Since a wide access interface with a pre-fetch buffer is provided, the wait state of a sequential Flash access is very close to zero.

WAIT [2:0]	Wait Status	Allowed HCLK Range
001	0	0MHz < HCLK ≦ 24MHz
010	1	24MHz < HCLK ≦ 48MHz
011	2	48MHz < HCLK ≦ 72MHz
Others	Reserved	Reserved

SRAM Booting Vector Register n – SBVTn (n = 0 ~3)

These registers specify the initial values of the Stack Point, Program Counter, NMI Handler address, and Hard Fault Handler address for the SRAM Booting mode.

Offset : 0x300 ~ 0x30C
Reset value : Various depending on the address offset

	31	30	29	28	27	26	25	24
	SBVTn							
Type/Reset	RWX	RWX	RWX	RWX	RWX	RWX	RWX	RWX
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	SBVTn							
Type/Reset	RWX	RWX	RWX	RWX	RWX	RWX	RWX	RWX
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	SBVTn							
Type/Reset	RWX	RWX	RWX	RWX	RWX	RWX	RWX	RWX
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	SBVTn							
Type/Reset	RWX	RWX	RWX	RWX	RWX	RWX	RWX	RWX

Bits	Field	Descriptions
[31:0]	SBVTn	SRAM Booting Vector n (n = 0 ~ 3) The SRAM Booting Vector 0 ~ 3 provides an SRAM booting capability for application debugging. The contents of the SBVTn registers are re-mapped into the addresses 0x0 to 0xC of the Flash Memory CODE area under the SRAM booting mode. Refer to the description of the VMCR register and BOOT1/BOOT0 boot pins. The following table shows the purpose and reset value of the SBVTn register. The reset value provides a fixed setting for program execution during the SRAM booting mode. These registers can be modified by the debugging tool in order to change the program execution setting. The reset values of the SBVTn register will be reloaded only by a power-on reset. Other reset sources will have no effect.

Name	Address Offset	Purpose Descriptions	Reset Value
SBVT0	0x300	Stack point	8 kB SRAM: 0x2000_2000 4 kB SRAM: 0x2000_1000 2 kB SRAM: 0x2000_0800
SBVT1	0x304	Program counter	0x2000_0101
SBVT2	0x308	NMI handler address	0x0000_0000
SBVT3	0x30C	Hard fault handler address	0x0000_0000

The access width of the registers SBVT0 ~SBVT3 must be a 32-bit access (Word access). 8 or 16 bits (Byte or Half-Word) access is not allowed.