

Technical Document

- [Application Note](#)
 - [HA0075E MCU Reset and Oscillator Circuits Application Note](#)

Features

CPU Features

- Operating voltage:
 - $f_{SYS}=4\text{MHz}$: 2.2V~5.5V
 - $f_{SYS}=8\text{MHz}$: 3.0V~5.5V
 - $f_{SYS}=12\text{MHz}$: 4.5V~5.5V
- Up to 0.33 μs instruction cycle with 12MHz system clock at $V_{DD}=5\text{V}$
- Sleep mode and wake-up functions to reduce power consumption
- Oscillator types:
 - External high frequency Crystal -- HXT
 - External RC -- ERC
 - Internal RC -- HIRC
 - External low frequency crystal -- LXT
- Four operational modes: Normal, Slow, Sleep
- Fully integrated internal 4MHz, 8MHz and 12MHz oscillator requires no external components
- 2048 \times 15 program memory
- 96 \times 8 data memory RAM
- Watchdog Timer function
- LIRC oscillator function for watchdog timer
- All instructions executed in one or two instruction cycles
- Table read instructions

- 63 powerful instructions
- 6-level subroutine nesting
- Bit manipulation instruction
- Low voltage reset function
- Wide range of available package types

Peripheral Features

- 21 bidirectional I/O lines
- 4 channel 12-bit ADC
- 1 channel 8-bit PWM
- Software controlled 4-SCOM lines LCD driver with 1/2 bias
- External interrupt input shared with an I/O line
- Two 8-bit programmable Timer/Event Counter with overflow interrupt and prescaler
- Time-Base function
- Programmable Frequency Divider - PFD
- Integrated DC 24V to 5V LDO regulator
- Buzzer and filament 5V to 24V output level shifter
- 24-bit shift register/latch for VFD panel driving 24 grid/segment outputs
- Integrated 3-line serial VFD interface for grid/segment display control
- 52-pin QFP package

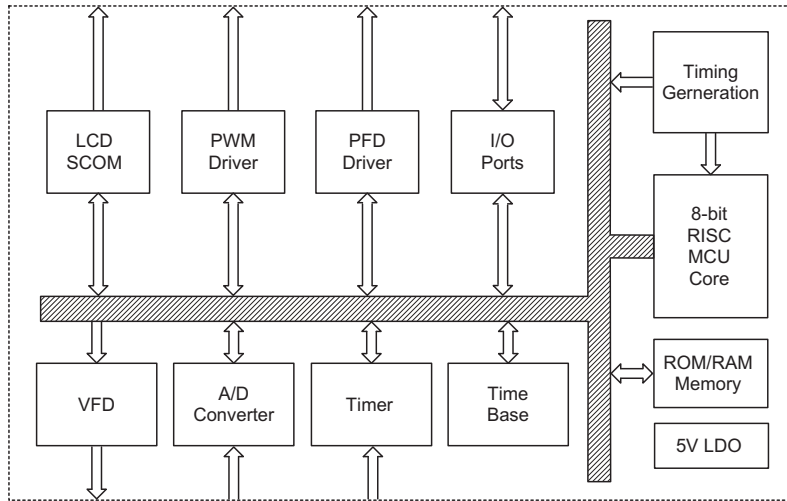
General Description

The Enhanced A/D MCUs are a series of 8-bit high performance, RISC architecture microcontrollers specifically designed for a wide range of applications. The usual Holtek microcontroller features of low power consumption, I/O flexibility, timer functions, oscillator options, power down and wake-up functions, watchdog timer and low voltage reset, combine to provide devices with a huge range of functional options while still main-

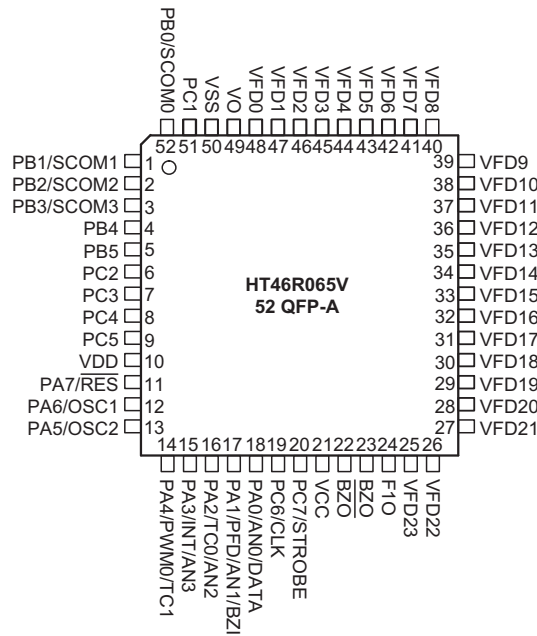
taining a high level of cost effectiveness. The fully integrated system oscillator HIRC, which requires no external components and which has three frequency selections, opens up a huge range of new application possibilities for these devices, some of which may include industrial control, consumer products, household appliances subsystem controllers, etc.

Block Diagram

The following block diagram illustrates the main functional blocks.



Pin Assignment



Pin Description

| Pin Name | Function | OPT | I/T | O/T | Description |
|------------------------------|-------------------------|--------------|-----|------|----------------------------------------------------------------------------------|
| PA0/AN0/DATA | PA0 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | AN0 | ADCR | AN | — | A/D channel 0 |
| | DATA | — | ST | — | VFD control interface |
| PA1/PFD/AN1/BZI | PA1 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | PFD | CTRL0 | — | CMOS | PFD output |
| | AN1 | ADCR | AN | — | A/D channel 1 |
| | BZI | — | ST | — | VFD control interface |
| PA2/TC0/AN2 | PA2 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | TC0 | — | ST | — | External Timer 0 clock input |
| | AN2 | ADCR | AN | — | A/D channel 2 |
| PA3/INT/AN3 | PA3 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | INT | — | ST | — | External interrupt input |
| | AN3 | ADCR | AN | — | A/D channel 3 |
| PA4/TC1/PWM0 | PA4 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | TC1 | — | ST | — | External Timer 1 clock input |
| | PWM0 | CTRL0 | — | CMOS | PWM output |
| PA5/OSC2 | PA5 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OSC2 | CO | — | OSC | Oscillator pin |
| PA6/OSC1 | PA6 | PAPU PAWK | ST | CMOS | General purpose I/O. Register enabled pull-up and wake-up. |
| | OSC1 | CO | OSC | — | Oscillator pin |
| PA7/ $\overline{\text{RES}}$ | PA7 | PAWK | ST | NMOS | General purpose I/O. Register enabled wake-up. |
| | $\overline{\text{RES}}$ | CO | ST | — | Reset input |
| PB0/SCOM0 | PB0 | PBPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | SCOM0 | SCOMC | — | SCOM | Software controlled 1/2 bias LCD COM |
| PB1/SCOM1 | PB1 | PBPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | SCOM1 | SCOMC | — | SCOM | Software controlled 1/2 bias LCD COM |
| PB2/SCOM2 | PB2 | PBPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | SCOM2 | SCOMC | — | SCOM | Software controlled 1/2 bias LCD COM |
| PB3/SCOM3 | PB3 | PBPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | SCOM3 | SCOMC | — | SCOM | Software controlled 1/2 bias LCD COM |
| PB4, PB5 | PBn | PBPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| PC0/F1 | PC0 | — | ST | CMOS | General purpose I/O. Register enabled pull-up. (not pin-out for this package) |
| | F1 | — | ST | — | Filament control Schmitt Trigger input. |

| Pin Name | Function | OPT | I/T | O/T | Description |
|------------------------------|-------------------------|------|-----|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PC1~PC5 | PCn | PCPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| PC6/CLK | PC6 | PCPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | CLK | — | ST | — | VFD control interface |
| PC7/STROBE | PC7 | PCPU | ST | CMOS | General purpose I/O. Register enabled pull-up. |
| | STROBE | — | ST | — | VFD control interface |
| VDD | VDD | — | PWR | — | Power supply |
| VSS | VSS | — | PWR | — | Ground |
| VFD23~VFD0 | VFDn | — | — | HV | High voltage grid/segment output for VFD panel |
| VCC | VCC | — | PWR | — | High voltage positive power supply for driving the VFD filament, F1O, BZO and BZO outputs. An external 10 μ F capacitor is recommended to be connected to ground on the PCB to reduce surge voltages. |
| VO | VO | — | — | PWR | LDO regulator output (5V). It's be recommend that connecting an external capacitor on PCB layout. |
| BZO, $\overline{\text{BZO}}$ | BZO | — | — | HV | High voltage buzzer complement output signals |
| | $\overline{\text{BZO}}$ | — | — | HV | |
| F1O | F1O | — | — | HV | High voltage filament output signal. |

Note: I/T: Input type; O/T: Output type
 OPT: Optional by configuration option (CO) or register option
 PWR: Power; CO: Configuration option
 ST: Schmitt Trigger input; CMOS: CMOS output; AN: analog input
 SCOM: Software controlled LCD COM
 HXT: High frequency crystal oscillator
 LXT: Low frequency crystal oscillator
 HV : high voltage output
 For VFD driver interface, the I/O function should only be configured as outputs.

Absolute Maximum Ratings

| | | | |
|-------------------------------|--------------------------------|-----------------------------|------------------------------------------------|
| Supply Voltage | $V_{SS}-0.3V$ to $V_{SS}+6.0V$ | Storage Temperature | -50°C to 125°C |
| Input Voltage | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature | -40°C to 85°C |
| I_{OL} Total | 100mA | I_{OH} Total | -100mA |
| Total Power Dissipation | 500mW | | |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------------------|-----------------|-----------------|-----------------------------------------------------------------------------|--------------------|------|--------------------|------|
| | | V _{DD} | V _{CC} | Conditions | | | | |
| V _{DD} | Operating Voltage | — | — | f _{SYS} =4MHz | 2.2 | — | 5.5 | V |
| | | | | f _{SYS} =8MHz | 3.0 | — | 5.5 | V |
| | | | | f _{SYS} =12MHz | 4.5 | — | 5.5 | V |
| I _{DD1} | Operating Current (HXT, HIRC, ERC) | 3V | — | No load, f _{SYS} =4MHz | — | 0.8 | 1.2 | mA |
| | | 5V | — | | — | 1.5 | 2.25 | mA |
| I _{DD2} | Operating Current (HXT, HIRC, ERC) | 3V | — | No load, f _{SYS} =8MHz | — | 1.4 | 2.1 | mA |
| | | 5V | — | | — | 2.8 | 4.2 | mA |
| I _{DD3} | Operating Current (HXT, HIRC, ERC) | 5V | — | No load, f _{SYS} =12MHz | — | 4 | 6 | mA |
| I _{DD4} | Operating Current (HIRC + LXT, Slow Mode) | 3V | — | No load, f _{SYS} =32768Hz (LXT on OSC1/OSC2, LVR disabled, LXTP=1) | — | 5 | 10 | μA |
| | | 5V | — | | — | 12 | 24 | μA |
| I _{STB1} | Standby Current (LIRC On, LXT Off) | 3V | — | No load, system HALT | — | — | 5 | μA |
| | | 5V | — | | — | — | 10 | μA |
| I _{STB2} | Standby Current (LIRC Off, LXT Off) | 3V | — | No load, system HALT | — | — | 1 | μA |
| | | 5V | — | | — | — | 2 | μA |
| I _{STB3} | Standby Current (LIRC Off, LXT On, LXTP=1) | 3V | — | No load, system HALT (LXT on OSC1/OSC2) | — | — | 5 | μA |
| | | 5V | — | | — | — | 10 | μA |
| V _{IL1} | Input Low Voltage for I/O, TCn and INT | — | — | — | 0 | — | 0.3V _{DD} | V |
| V _{IH1} | Input High Voltage for I/O, TCn and INT | — | — | — | 0.7V _{DD} | — | V _{DD} | V |
| V _{IL2} | Input Low Voltage (\overline{RES}) | — | — | — | 0 | — | 0.4V _{DD} | V |
| V _{IH2} | Input High Voltage (\overline{RES}) | — | — | — | 0.9V _{DD} | — | V _{DD} | V |
| V _{LVR1} | Low Voltage Reset 1 | — | — | VLVR=4.2V | 3.98 | 4.2 | 4.42 | V |
| V _{LVR2} | Low Voltage Reset 2 | — | — | VLVR=3.15V | 2.98 | 3.15 | 3.32 | V |
| V _{LVR3} | Low Voltage Reset 3 | — | — | VLVR=2.1V | 1.98 | 2.1 | 2.22 | V |
| I _{OL1} | I/O Port Sink Current | 3V | — | V _{OL} =0.1V _{DD} | 4 | 8 | — | mA |
| | | 5V | — | | 10 | 20 | — | mA |
| I _{OH} | I/O Port Source Current | 3V | — | V _{OH} =0.9V _{DD} | -2 | -4 | — | mA |
| | | 5V | — | | -5 | -10 | — | mA |
| I _{OL2} | PA7 Sink Current | 5V | — | V _{OL} =0.1V _{DD} | 2 | 3 | — | mA |
| R _{PH} | Pull-high Resistance | 3V | — | — | 20 | 60 | 100 | kΩ |
| | | 5V | — | — | 10 | 30 | 50 | kΩ |
| I _{SCOM} | SCOM Operating Current | 5V | — | SCOMC, ISEL[1:0]=00 | 17.5 | 25.0 | 32.5 | μA |
| | | | | SCOMC, ISEL[1:0]=01 | 35 | 50 | 65 | μA |
| | | | | SCOMC, ISEL[1:0]=10 | 70 | 100 | 130 | μA |
| | | | | SCOMC, ISEL[1:0]=11 | 140 | 200 | 260 | μA |

| Symbol | Parameter | Test Conditions | | | Min. | Typ. | Max. | Unit |
|-------------------|-----------------------------------------------------------------|-----------------|-----------------|---------------------------------------------------|-------|-------|-------|-----------------|
| | | V _{DD} | V _{CC} | Conditions | | | | |
| V _{SCOM} | V _{DD} /2 Voltage for LCD COM | 5V | — | No load | 0.475 | 0.500 | 0.525 | V _{DD} |
| V _{CC} | VFD, F10, BZO and $\overline{\text{BZO}}$ Output Supply Voltage | — | — | — | 12 | — | 24 | V |
| I _{CC1} | Logic Operating Current 1 | 5V | 18V | No load, VFD outputs, all output low, CLK=100kHz | — | 70 | 110 | μA |
| | | | 24V | | — | 90 | 135 | μA |
| I _{CC2} | Logic Operating Current 2 | 5V | 18V | No load, VFD outputs, all output high, CLK=100kHz | — | 70 | 110 | μA |
| | | | 24V | | — | 90 | 135 | μA |
| I _{CC3} | Buzzer Operating Current | 5V | 18V | No load, BZI input 50kHz | — | 100 | 150 | μA |
| | | | 24V | | — | 120 | 180 | μA |
| I _{CC4} | Filament Operating Current | 5V | 18V | No load, F1 input 50kHz | — | 80 | 120 | μA |
| | | | 24V | | — | 100 | 150 | μA |
| I _{STB4} | Standby Current (LDO Always On, WDT Enable/Disable) | 5V | 18V | No load | — | 70 | 105 | μA |
| | | | 24V | | — | 90 | 135 | μA |
| I _{OL2} | F10 Sink Current | 5V | 18V | V _{OL} = 0.1V _{CC} | 2.5 | 5.0 | — | mA |
| | | | 24V | | 5.0 | 10.0 | — | mA |
| I _{OH2} | F10 Source Current | 5V | 18V | V _{OH} = 0.9V _{CC} | -15 | -30 | — | mA |
| | | | 24V | | -22 | -25 | — | mA |
| I _{OL3} | BZO/ $\overline{\text{BZO}}$ Sink Current | 5V | 18V | V _{OL} = 0.1V _{CC} | 15 | 30 | — | mA |
| | | | 24V | | 25 | 50 | — | mA |
| I _{OH3} | BZO/ $\overline{\text{BZO}}$ Source Current | 5V | 18V | V _{OH} = 0.9V _{CC} | -15 | -30 | — | mA |
| | | | 24V | | -25 | -50 | — | mA |
| I _{OL4} | Grid/Segment Sink Current | 5V | 18V | V _{OL} = 0.1V _{CC} | 2.5 | 5.0 | — | mA |
| | | | 24V | | 5.0 | 10.0 | — | mA |
| I _{OH4} | Grid/Segment Source Current | 5V | 18V | V _{OH} = 0.9V _{CC} | -6 | -12 | — | mA |
| | | | 24V | | -10 | -20 | — | mA |

Note: The standby current (I_{STB1}~I_{STB3}) and I_{DD4} are measured with all I/O pins in input mode and tied to V_{DD}.

A.C. Characteristics

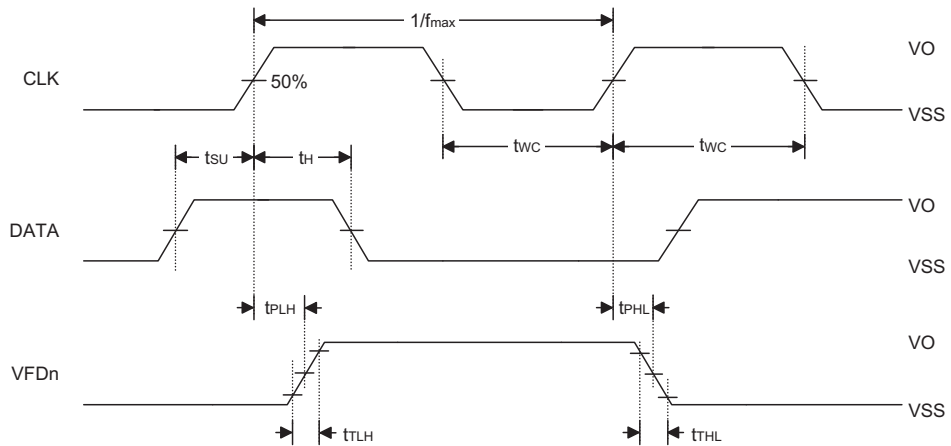
Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|--------------------|--------------------------------|-----------------|---------------------------------------|------|-------|-------|------------------|
| | | V _{DD} | Conditions | | | | |
| f _{sys} | System Clock | — | 2.2V~5.5V | 32 | — | 4000 | kHz |
| | | | 3.0V~5.5V | 32 | — | 8000 | kHz |
| | | | 4.5V~5.5V | 32 | — | 12000 | kHz |
| f _{HIRC} | System Clock (HIRC) | 3V/5V | Ta=25°C | -2% | 4 | +2% | MHz |
| | | 3V/5V | Ta=25°C | -2% | 8 | +2% | MHz |
| | | 5V | Ta=25°C | -2% | 12 | +2% | MHz |
| | | 3V/5V | Ta=0~70°C | -5% | 4 | +5% | MHz |
| | | 3V/5V | Ta=0~70°C | -5% | 8 | +5% | MHz |
| | | 5V | Ta=0~70°C | -5% | 12 | +5% | MHz |
| | | 2.2V~3.6V | Ta=0~70°C | -8% | 4 | +8% | MHz |
| | | 3.0V~5.5V | Ta=0~70°C | -8% | 4 | +8% | MHz |
| | | 3.0V~5.5V | Ta=0~70°C | -8% | 8 | +8% | MHz |
| | | 4.5V~5.5V | Ta=0~70°C | -8% | 12 | +8% | MHz |
| | | 2.2V~3.6V | Ta= -40°C~85°C | -12% | 4 | +12% | MHz |
| | | 3.0V~5.5V | Ta= -40°C~85°C | -12% | 4 | +12% | MHz |
| | | 3.0V~5.5V | Ta= -40°C~85°C | -12% | 8 | +12% | MHz |
| | | 4.5V~5.5V | Ta= -40°C~85°C | -12% | 12 | +12% | MHz |
| f _{LXT} | System Clock (LXT) | — | — | — | 32768 | — | Hz |
| f _{TIMER} | Timer Input Frequency (TCn) | — | 2.2V~5.5V | 0 | — | 4000 | kHz |
| | | | 3.0V~5.5V | 0 | — | 8000 | kHz |
| | | | 4.5V~5.5V | 0 | — | 12000 | kHz |
| f _{LIRC} | LIRC Oscillator | 3V | — | 5 | 10 | 15 | kHz |
| | | 5V | — | 6.5 | 13 | 19.5 | kHz |
| t _{RES} | External Reset Low Pulse Width | — | — | 1 | — | — | μs |
| t _{SST} | System Start-up time Period | — | For HXT/LXT | — | 1024 | — | t _{sys} |
| | | | For ERC/IRC (By configuration option) | — | 2 | — | t _{sys} |
| t _{INT} | Interrupt Pulse Width | — | — | 1 | — | — | μs |
| t _{LVR} | Low Voltage Width to Reset | — | — | 0.25 | 1 | 2 | ms |
| RESTD | Reset Delay Time | — | — | — | 100 | — | ms |

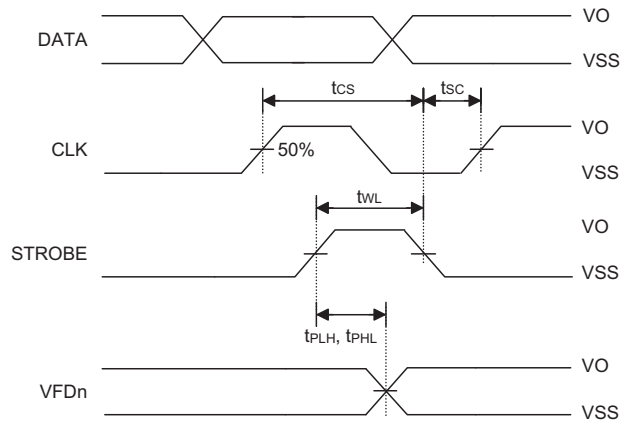
| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|----------------------------------------|--------------------------------------------------|-----------------|----------------------|------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Time (Clock to VFD Output) | — | V _{CC} =15V | — | 100 | 200 | ns |
| | Propagation Delay Time (Strobe to VFD Output) | | | — | 100 | 200 | ns |
| t _{THL} , t _{TLH} | Transition Time | — | V _{CC} =15V | — | 40 | 80 | ns |
| t _{SU} | Data Setup Time | — | V _{CC} =15V | — | 10 | 20 | ns |
| t _{CS} | Setup Time (Clock to Strobe) | — | V _{CC} =15V | — | 10 | 20 | ns |
| t _H | Hold Time (Data to Clock) | — | V _{CC} =15V | — | 10 | 20 | ns |
| t _{SC} | Hold Time (Clock to Strobe) | — | V _{CC} =15V | — | 75 | 150 | ns |
| t _r , t _f | Clock Input Rise or Fall Time | — | V _{CC} =15V | — | — | 20 | ns |
| t _{WC} | Clock Pulse Width | — | V _{CC} =15V | — | 40 | 83 | ns |
| t _{WL} | Strobe Pulse Width | — | V _{CC} =15V | — | 35 | 70 | ns |
| f _{max} | Maximum Clock Input Frequency | — | V _{CC} =15V | — | 8 | — | MHz |

- Note:
1. t_{SYS}=1/f_{SYS}
 2. *For f_{ERC}, as the resistor tolerance will influence the frequency a precision resistor is recommended.
 3. To maintain the accuracy of the internal HIRC oscillator frequency, a 0.1μF decoupling capacitor should be connected between VDD and VSS and located as close to the device as possible.

A.C. Waveforms



Data Propagation Delays, Setup and Hold Times



Strobe Propagation Delays, Setup and Hold Times

ADC Characteristics

Ta=25°C

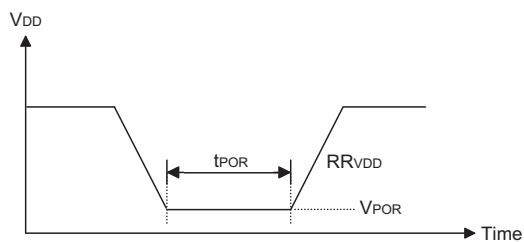
| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------------------------------|-----------------|------------------------|------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| DNL | A/C Differential Non-Linearity | 3V | t _{AD} =0.5μs | -2 | — | 2 | LSB |
| | | 5V | | | | | |
| INL | ADC Integral Non-Linearity | 3V | t _{AD} =0.5μs | -4 | — | 4 | LSB |
| | | 5V | | | | | |
| I _{ADC} | Additional Power Consumption if A/D Converter is Used | 3V | — | — | 0.5 | 0.75 | mA |
| | | 5V | | — | 1.0 | 1.5 | mA |

LDO Characteristic

| Symbol | Parameter | Test Conditions | | | Min. | Typ. | Max. | Unit |
|------------------|----------------------------|-----------------|-----------------|-------------------------------------------------------------------------|------|------|------|------|
| | | V _{DD} | V _{CC} | Conditions | | | | |
| V _O | LDO Output Voltage | — | — | — | 4.7 | 5.0 | 5.3 | V |
| I _{OUT} | Maximum LDO Output Current | — | — | For V _{CC} ≥5V | 10 | — | — | mA |
| ΔVLNR | Line Regulation | — | — | V _{IN} =(V _{OUT} +0.1V) to 24V, I _{OUT} =1mA | — | 0.2 | — | %/V |
| ΔVLDR | Load Regulation | — | — | I _{OUT} =100μA to 20mA, C _{OUT} =10pF | — | 0.1 | 0.2 | %/mA |
| VDRO | Dropout Voltage | — | — | I _{OUT} =1mA | 25 | 30 | 35 | mV |

Power-on Reset Characteristics

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------------------------------------------------|-----------------|------------|-------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| V _{POR} | VDD Start Voltage to Ensure Power-on Reset | — | — | — | — | 100 | mV |
| RR _{VDD} | VDD raising rate to Ensure Power-on Reset | — | — | 0.035 | — | — | V/ms |
| t _{POR} | Minimum Time for VDD Stays at V _{POR} to Ensure Power-on Reset | — | — | 1 | — | — | ms |



System Architecture

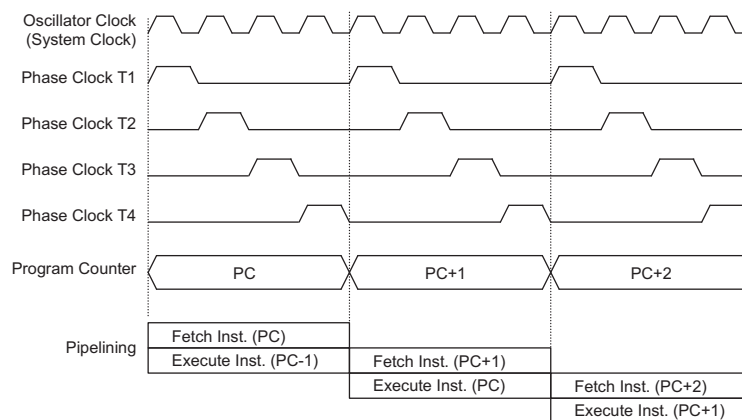
A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to the internal system architecture. The range of devices take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all operations of the instruction set. It carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility.

Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

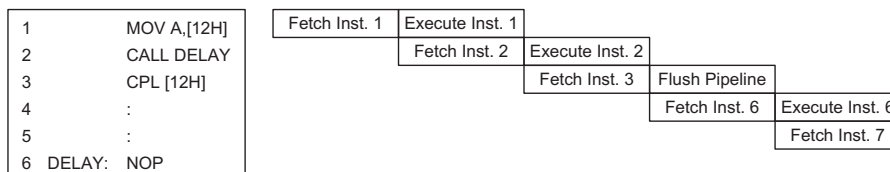
For instructions involving branches, such as jump or call instructions, two instruction cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.

Clocking and Pipelining

The main system clock, derived from either a Crystal/Resonator or RC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The



System Clocking and Pipelining



Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demand a jump to a non-consecutive Program Memory address. Note that the Program Counter width varies with the Program Memory capacity depending upon which device is selected. However, it must be noted that only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by user.

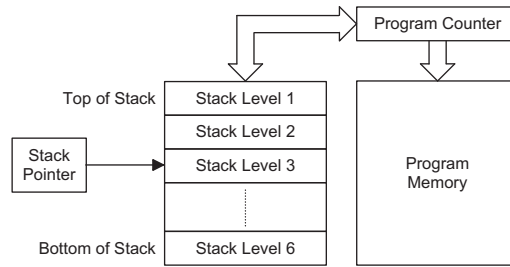
When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly, however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory, that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted.

The lower byte of the Program Counter is fully accessible under program control. Manipulating the PCL might cause program branching, so an extra cycle is needed to pre-fetch. Further information on the PCL register can be found in the Special Function Register section.

Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack is neither part of the Data or Program Memory space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, SP, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.



If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

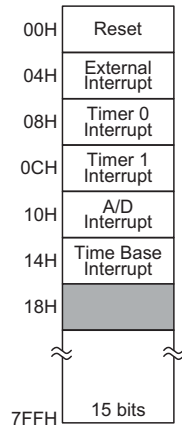
- Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA
- Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA
- Rotation RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC
- Increment and Decrement INCA, INC, DECA, DEC
- Branch decision, JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI

Program Memory

The Program Memory is the location where the user code or program is stored. The device is supplied with One-Time Programmable, OTP, memory where users can program their application code into the device. By using the appropriate programming tools, OTP devices offer users the flexibility to freely develop their applications which may be useful during debug or for products requiring frequent upgrades or program changes.

Structure

The Program Memory has a capacity of 2K×15. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by separate table pointer registers.



Program Memory Structure

Special Vectors

Within the Program Memory, certain locations are reserved for special usage such as reset and interrupts.

- **Reset Vector**
This vector is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.
- **External interrupt vector**
This vector is used by the external interrupt. If the external interrupt pin on the device receives an edge transition, the program will jump to this location and begin execution if the external interrupt is enabled and the stack is not full. The external interrupt active edge transition type, whether high to low, low to high or both is specified in the CTRL1 register.

- **Timer/Event 0/1/2 counter interrupt vector**
This internal vector is used by the Timer/Event Counters. If a Timer/Event Counter overflow occurs, the program will jump to its respective location and begin execution if the associated Timer/Event Counter interrupt is enabled and the stack is not full.
- **Time base interrupt vector**
This internal vector is used by the internal Time Base. If a Time Base overflow occurs, the program will jump to this location and begin execution if the Time Base counter interrupt is enabled and the stack is not full.
- **AD conversion interrupt**
This internal vector is used by the A/D converter. When an A/D conversion cycle is complete, the program will jump to this location and begin execution if the A/D interrupt is enabled and the stack is not full.

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the lower order address of the look up data to be retrieved in the table pointer register, TBLP. This register defines the lower 8-bit address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the current Program Memory page or last Program Memory page using the "TABRDC[m]" or "TABRDL [m]" instructions, respectively. When these instructions are executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register. Any unused bits in this transferred higher order byte will be read as "0".

The following diagram illustrates the addressing/data flow of the look-up table:

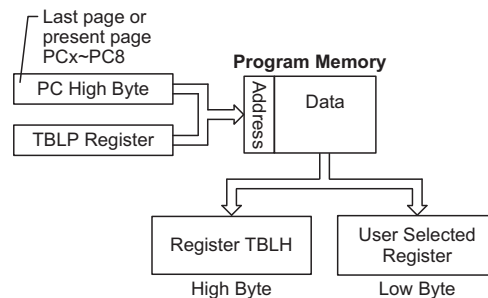


Table Program Example

The accompanying example shows how the table pointer and table data is defined and retrieved from the device. This example uses raw table data located in the last page which is stored there using the ORG statement. The value at this ORG statement is "700H" which refers to the start address of the last page within the 1K Program Memory of the HT46R065V microcontrollers. The table pointer is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "706H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address of the present page if the "TABRDC [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRDL [m]" instruction is executed.

Because the TBLH register is a read-only register and cannot be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use the table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

• Table Read Program Example

```

tempreg1 db ?           ; temporary register #1
tempreg2 db ?           ; temporary register #2
:
:

mov a,06h                ; initialise table pointer - note that this address
                        ; is referenced

mov tblp,a               ; to the last page or present page
:
:

tabrdl tempreg1          ; transfers value in table referenced by table pointer
                        ; to tempreg1
                        ; data at prog. memory address "706H" transferred to
                        ; tempreg1 and TBLH

dec tblp                 ; reduce value of table pointer by one

tabrdl tempreg2          ; transfers value in table referenced by table pointer
                        ; to tempreg2
                        ; data at prog.memory address "705H" transferred to
                        ; tempreg2 and TBLH
                        ; in this example the data "1AH" is transferred to
                        ; tempreg1 and data "0FH" to register tempreg2
                        ; the value "00H" will be transferred to the high byte
                        ; register TBLH
:
:

org 700h                 ; sets initial address of last page

dc 00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
:
:

```

| Instruction | Table Location Bits | | | | | | | | | | |
|-------------|---------------------|-----|-----|----|----|----|----|----|----|----|----|
| | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| TABRDC [m] | PC10 | PC9 | PC8 | @7 | @6 | @5 | @4 | @3 | @2 | @1 | @0 |
| TABRDL [m] | 1 | 1 | 1 | @7 | @6 | @5 | @4 | @3 | @2 | @1 | @0 |

Table Location

Note: PC10~PC8: Current Program Counter bits
 @7~@0: Table Pointer TBLP bits

Data Memory

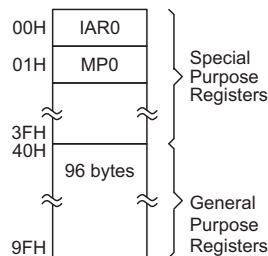
The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

Structure

Divided into two sections, the first of these is an area of RAM where special function registers are located. These registers have fixed locations and are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control.

The two sections of Data Memory, the Special Purpose and General Purpose Data Memory are located at consecutive locations. All are implemented in RAM and are 8 bits wide but the length of each memory section is dictated by the type of microcontroller chosen. The start address of the Data Memory for all devices is the address "00H".

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user program for both read and write operations. By using the "SET [m].i" and "CLR [m].i" instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.



Data Memory Structure

Note: Most of the Data Memory bits can be directly manipulated using the "SET [m].i" and "CLR [m].i" with the exception of a few dedicated bits. The Data Memory can also be accessed through the memory pointer registers.

Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value "00H".

| | |
|-----|--------|
| 00H | IAR0 |
| 01H | MP0 |
| 02H | IAR1 |
| 03H | MP1 |
| 04H | |
| 05H | ACC |
| 06H | PCL |
| 07H | TBLP |
| 08H | TBLH |
| 09H | WDTS |
| 0AH | STATUS |
| 0BH | INTC0 |
| 0CH | TMR0 |
| 0DH | TMR0C |
| 0EH | TMR1 |
| 0FH | TMR1C |
| 10H | PA |
| 11H | PAC |
| 12H | PAPU |
| 13H | PAWK |
| 14H | PB |
| 15H | PBC |
| 16H | PBPU |
| 17H | PC |
| 18H | PCC |
| 19H | PCPU |
| 1AH | CTRL0 |
| 1BH | CTRL1 |
| 1CH | SCOMC |
| 1DH | |
| 1EH | INTC1 |
| 1FH | PWM0 |
| 20H | ADRL |
| 21H | ADRH |
| 22H | ADCR |
| 23H | ACSR |
| 24H | |
| 25H | |
| 26H | |
| 27H | |
| 28H | |
| 29H | |
| 2AH | |
| 2BH | |
| 2CH | |
| 2DH | |
| 2EH | |
| 2FH | |
| 30H | |
| 31H | |
| 32H | |
| ... | |
| 3FH | |

■ : Unused, read as "00"

Special Purpose Data Memory

Special Function Registers

To ensure successful operation of the microcontroller, certain internal registers are implemented in the Data Memory area. These registers ensure correct operation of internal functions such as timers, interrupts, etc., as well as external functions such as I/O data control. Any unused Data Memory locations between these special function registers and the point where the General Purpose Memory begins is reserved and attempting to read data from these locations will return a value of "00H".

Indirect Addressing Registers – IAR0, IAR1

The Indirect Addressing Registers, IAR0 and IAR1, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0 and IAR1 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointer, MP0 or MP1. Acting as a pair, IAR0 with MP0 and IAR1 with MP1 can together access data from the Data Memory. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

Memory Pointers – MP0, MP1

Two Memory Pointers, known as MP0 and MP1 are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to indirectly address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to, is the address specified by the related Memory Pointer. The following example shows how to clear a section of four Data Memory locations already defined as locations adres1 to adres4.

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

• Indirect Addressing Program Example

```

data .section 'data'
adres1 db ?
adres2 db ?
adres3 db ?
adres4 db ?
block db ?
code .section at 0 code
org 00h

start:
    mov a,04h                ; setup size of block
    mov block,a
    mov a,offset adres1     ; Accumulator loaded with first RAM address
    mov mp0,a               ; setup memory pointer with first RAM address

loop:
    clr IAR0                ; clear the data at address defined by MP0
    inc mp0                 ; increment memory pointer
    sdz block               ; check if last memory location has been cleared
    jmp loop

continue:

```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the interrupt routine can change the status register, precautions must be taken to correctly save it. Note that bits 0–3 of the STATUS register are both readable and writeable bits.

• STATUS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|----|-----|-----|-----|-----|-----|
| Name | — | — | TO | PDF | OV | Z | AC | C |
| R/W | — | — | R | R | R/W | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | x | x | x | x |

"x" unknown

- Bit 7, 6 Unimplemented, read as "0"
- Bit 5 **TO:** Watchdog Time-Out flag
0: After power up or executing the "CLR WDT" or "HALT" instruction
1: A watchdog time-out occurred.
- Bit 4 **PDF:** Power down flag
0: After power up or executing the "CLR WDT" instruction
1: By executing the "HALT" instruction
- Bit 3 **OV:** Overflow flag
0: no overflow
1: an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa.
- Bit 2 **Z:** Zero flag
0: The result of an arithmetic or logical operation is not zero
1: The result of an arithmetic or logical operation is zero
- Bit 1 **AC:** Auxiliary flag
0: no auxiliary carry
1: an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction
- Bit 0 **C:** Carry flag
0: no carry-out
1: an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation
C is also affected by a rotate through carry instruction.

Input/Output Ports and Control Registers

Within the area of Special Function Registers, the port PA, PB, etc data I/O registers and their associated control register PAC, PBC, etc play a prominent role. These registers are mapped to specific addresses within the Data Memory as shown in the Data Memory table. The data I/O registers, are used to transfer the appropriate output or input data on the port. The control registers specifies which pins of the port are set as inputs and which are set as outputs. To setup a pin as an input, the corresponding bit of the control register must be set high, for an output it must be set low. During program initialisation, it is important to first setup the control registers to specify which pins are outputs and which are inputs before reading data from or writing data to the I/O ports. One flexible feature of these registers is the ability to directly program single bits using the "SET [m].i" and "CLR [m].i" instructions. The ability to change I/O pins from output to input and vice versa by manipulating specific bits of the I/O control registers during normal program operation is a useful feature of these devices.

System Control Registers – CTRL0, CTRL1

These registers are used to provide control over various internal functions. Some of these include the PFD control, PWM control, certain system clock options, the LXT Oscillator low power control, external Interrupt edge trigger type, Watchdog Timer enable function, Time Base function division ratio, and the LXT oscillator enable control.

Wake-up Function Register – PAWK

When the microcontroller enters the Sleep Mode, various methods exist to wake the device up and continue with normal operation. One method is to allow a falling edge on the I/O pins to have a wake-up function. This register is used to select which Port A I/O pins are used to have this wake-up function.

Pull-high Registers – PAPU, PBPU, PCPU

The I/O pins, if configured as inputs, can have internal pull-high resistors connected, which eliminates the need for external pull-high resistors. This register selects which I/O pins are connected to internal pull-high resistors.

Software COM Register – SCOMC

The pins PB0~PB3 on Port B can be used as SCOM lines to drive an external LCD panel. To implement this function, the SCOMC register is used to setup the correct bias voltages on these pins.

• CTRL0 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|-------|--------|---|-------|------|-------|--------|
| Name | — | PFDCS | PWMSEL | — | PWMC0 | PFDC | LXTLP | CLKMOD |
| R/W | — | R/W | R/W | — | R/W | R/W | R/W | R/W |
| POR | — | 0 | 0 | — | 0 | 0 | 0 | 0 |

Bit 7 Unimplemented, read as "0"

Bit 6 **PFDCS**: PFD clock source
0: timer0
1: timer1

Bit 5 **PWMSEL**: PWM type selection
0: 6+2
1: 7+1

Bit 4 Unimplemented, read as "0"

Bit 3 **PWMC0**: I/O or PWM0
0: I/O
1: PWM0

Bit 2 **PFDC**: I/O or PFD
0: I/O
1: PFD

Bit 1 **LXTLP**: LXT oscillator low power control function
0: LXT Oscillator quick start-up mode
1: LXT Oscillator Low Power Mode

Bit 0 **CLKMOD**: system clock mode selection.
0: High speed - HIRC used as system clock
1: Low speed - LXT used as system clock, HIRC oscillator stopped.
For the selections are only valid if the oscillator configuration options have selected the HIRC+LXT.

Note: If PWM0 output is selected by PWMC0 bit, f_{TP} comes always from f_{SYS} .
(f_{TP} is the clock source for timer0, time base and PWM)

• CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | INTEG1 | INTEG0 | TBSEL1 | TBSEL0 | WDTEN3 | WDTEN2 | WDTEN1 | WDTEN0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Bit 7, 6 **INTEG1, INTEG0**: External interrupt edge type
00: disable
01: rising edge trigger
10: falling edge trigger
11: dual edge trigger

Bit 5, 4 **TBSEL1, TBSEL0**: Time base period selection
00: $2^{10} \times (1/f_{TP})$
01: $2^{11} \times (1/f_{TP})$
10: $2^{12} \times (1/f_{TP})$
11: $2^{13} \times (1/f_{TP})$

Bit 3~0 **WDTEN3, WDTE2, WDTE1, WDTE0**: WDT function enable
1010: WDT disabled
Other values: WDT enabled - Recommended value is 0101

If the "watchdog timer enable" is configuration option is selected, then the watchdog timer will always be enabled and the WDTE3~WDTE0 control bits will have no effect.

Note: The WDT is only disabled when both the WDT configuration option is disabled and when bits WDTE3~WDTE0=1010.

The WDT is enabled when either the WDT configuration option is enabled or when bits WDTE3~WDTE0≠1010.

Oscillator

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator selections and operation are selected through a combination of configuration options and registers.

System Oscillator Overview

In addition to being the source of the main system clock the oscillators also provide clock sources for the Watchdog Timer and Time Base functions. External oscillators requiring some external components as well as a two fully integrated internal oscillators, requiring no external components, are provided to form a wide range of both fast and slow system oscillators.

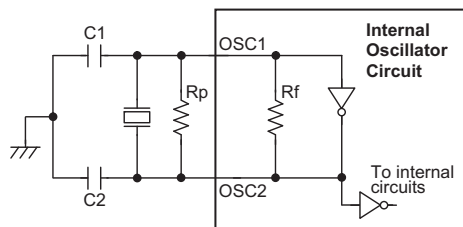
| Type | Name | Freq. | Pins |
|----------------------------|------|---------------|-----------|
| External Crystal | HXT | 400kHz~12MHz | OSC1/OSC2 |
| External RC | ERC | 400kHz~12MHz | OSC1 |
| Internal High Speed RC | HIRC | 4, 8 or 12MHz | — |
| External Low Speed Crystal | LXT | 32768Hz | OSC1/OSC2 |
| Internal Low Speed RC | LIRC | 13kHz | — |

System Clock Configurations

There are five system oscillators. Three high speed oscillators and two low speed oscillators. The high speed oscillators are the external crystal/ceramic oscillator - HXT, the external - ERC, and the internal RC oscillator - HIRC. The two low speed oscillator are the external 32768Hz oscillator - LXT and the internal 13kHz ($V_{DD}=5V$) oscillator - LIRC.

External Crystal/Resonator Oscillator – HXT

The simple connection of a crystal across OSC1 and OSC2 will create the necessary phase shift and feedback for oscillation. However, for some crystals and



- Note:
1. R_p is normally not required. C1 and C2 are required.
 2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7pF.

Crystal/Resonator Oscillator – HXT

most resonator types, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer's specification.

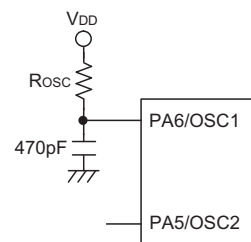
| Crystal Oscillator C1 and C2 Values | | |
|-------------------------------------|-------|-------|
| Crystal Frequency | C1 | C2 |
| 12MHz | 8pF | 10pF |
| 8MHz | 8pF | 10pF |
| 4MHz | 8pF | 10pF |
| 1MHz | 100pF | 100pF |

Note: C1 and C2 values are for guidance only.

Crystal Recommended Capacitor Values

External RC Oscillator – ERC

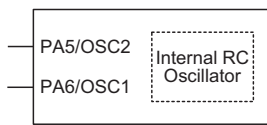
Using the ERC oscillator only requires that a resistor, with a value between 24k Ω and 1.5M Ω , is connected between OSC1 and VDD, and a capacitor is connected between OSC and ground, providing a low cost oscillator configuration. It is only the external resistor that determines the oscillation frequency; the external capacitor has no influence over the frequency and is connected for stability purposes only. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. As a resistance/frequency reference point, it can be noted that with an external 120K resistor connected and with a 5V voltage power supply and temperature of 25 degrees, the oscillator will have a frequency of 4MHz within a tolerance of 2%. Here only the OSC1 pin is used, which is shared with I/O pin PA6, leaving pin PA5 free for use as a normal I/O pin.



External RC Oscillator – ERC

Internal RC Oscillator – HIRC

The internal RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has three fixed frequencies of either 4MHz, 8MHz or 12MHz. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. As a result, at a power supply of either 3V or 5V and at a temperature of 25 degrees, the fixed oscillation frequency of 4MHz, 8MHz or 12MHz will have a tolerance within 2%. Note that if this internal system clock option is selected, as it requires no external pins for its operation, I/O pins PA5 and PA6 are free for use as normal I/O pins.

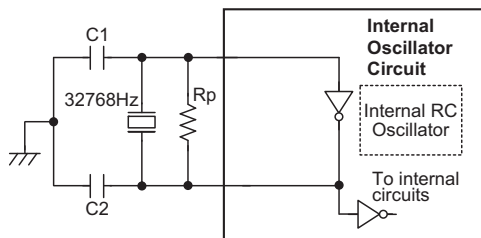


Note: PA5/PA6 used as normal I/Os

Internal RC Oscillator – HIRC

External 32768Hz Crystal Oscillator – LXT

When the microcontroller enters the Sleep Mode, the system clock is switched off to stop microcontroller activity and to conserve power. However, in many microcontroller applications it may be necessary to keep the internal timers operational even when the microcontroller is in the Power-down Mode. To do this, another clock, independent of the system clock, must be provided. To do this a configuration option exists to allow a high speed oscillator to be used in conjunction with a low speed oscillator, known as the LXT oscillator. The LXT oscillator is implemented using a 32768Hz crystal connected to pins OSC1/OSC2. However, for some crystals, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer’s specification. The external parallel feedback resistor, Rp, is required. The LXT oscillator must be used together with the HIRC oscillator.



Note: 1. Rp, C1 and C2 are required.
2. Although not shown pins have a parasitic capacitance of around 7pF.

External LXT Oscillator

| LXT Oscillator C1 and C2 Values | | |
|-----------------------------------------------------------------------------------|-----|------|
| Crystal Frequency | C1 | C2 |
| 32768Hz | 8pF | 10pF |
| Note: 1. C1 and C2 values are for guidance only. 2. Rp=5M~10MΩ is recommended. | | |

32768 Hz Crystal Recommended Capacitor Values

LXT Oscillator Low Power Function

The LXT oscillator can function in one of two modes, the Quick Start Mode and the Low Power Mode. The mode selection is executed using the LXTLP bit in the CTRL0 register.

| LXTLP Bit | LXT Mode |
|-----------|-------------|
| 0 | Quick Start |
| 1 | Low-power |

After power on the LXTLP bit will be automatically cleared to zero ensuring that the LXT oscillator is in the Quick Start operating mode. In the Quick Start Mode the LXT oscillator will power up and stabilise quickly. However, after the LXT oscillator has fully powered up it can be placed into the Low-power mode by setting the LXTLP bit high. The oscillator will continue to run but with reduced current consumption, as the higher current consumption is only required during the LXT oscillator start-up. In power sensitive applications, such as battery applications, where power consumption must be kept to a minimum, it is therefore recommended that the application program sets the LXTLP bit high about 2 seconds after power-on.

It should be noted that, no matter what condition the LXTLP bit is set to, the LXT oscillator will always function normally, the only difference is that it will take more time to start up if in the Low-power mode.

Internal Low Speed Oscillator – LIRC

The LIRC is a fully self-contained free running on-chip RC oscillator with a typical frequency of 13kHz at 5V requiring no external components. When the device enters the Sleep Mode, the system clock will stop running but the WDT oscillator continues to free-run and to keep the watchdog active. However, to preserve power in certain applications the LIRC can be disabled via a configuration option.

Operating Modes

By using the LXT low frequency oscillator in combination with a high frequency oscillator, the system can be selected to operate in a number of different modes. These Modes are Normal, Slow and Sleep.

Mode Types and Selection

The higher frequency oscillators provide higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow oscillators, the device has the flexibility to optimise the performance/power ratio, a feature especially important in power sensitive portable applications.

For the devices, if the LXT oscillator is used then the internal RC oscillator, HIRC, must be used as the high frequency oscillator. If the HXT or the ERC oscillator is chosen as the high frequency system clock then the LXT oscillator cannot be used for sharing the same pins. The CLKMOD bit in the CTRL0 register can be used to switch the system clock from the high speed HIRC oscillator to the low speed LXT oscillator. When the HALT instruction is executed and the device enters the Sleep Mode the LXT oscillator will always continue to run. For these devices the LXT crystal is connected to the OSC1/OSC2 pins and LXT will always run.

Note that CLKMOD is only valid in HIRC+LXT oscillator configuration.

| Operating Mode | OSC1/OSC2 Configuration | | | | |
|----------------|-------------------------|------|------|------------|-----|
| | HXT | ERC | HIRC | HIRC + LXT | |
| | | | | HIRC | LXT |
| Normal | Run | Run | Run | Run | Run |
| Slow | — | — | — | Stop | Run |
| Sleep | Stop | Stop | Stop | Stop | Run |

Note: "—" unimplemented

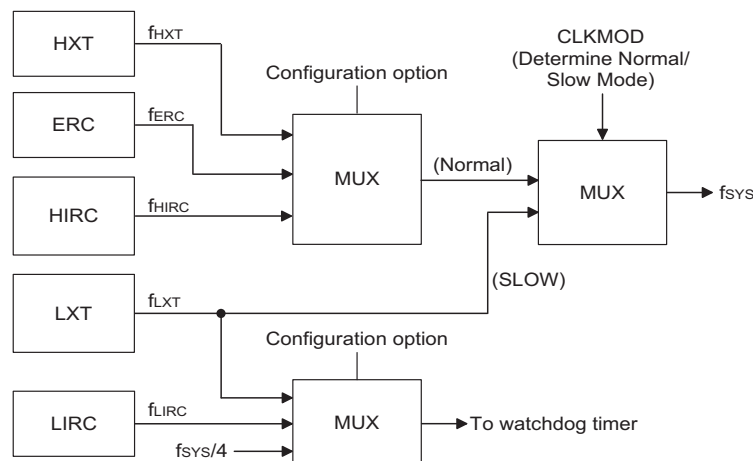
Operating Mode Control

Mode Switching

The devices are switched between one mode and another using a combination of the CLKMOD bit in the CTRL0 register and the HALT instruction. The CLKMOD bit chooses whether the system runs in either the Normal or Slow Mode by selecting the system clock to be sourced from either a high or low frequency oscillator. The HALT instruction forces the system into either the Sleep Mode, depending upon whether the LXT oscillator is running or not. The HALT instruction operates independently of the CLKMOD bit condition.

When a HALT instruction is executed and the LXT oscillator is not running, the system enters the Sleep mode the following conditions exist:

- The system oscillator will stop running and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the WDT or LXT oscillator. The WDT will stop if its clock source originates from the system clock.
- The I/O ports will maintain their present condition.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.



System Clock Configurations

Standby Current Considerations

As the main reason for entering the Sleep Mode is to keep the current consumption of the MCU to as low a value as possible, perhaps only in the order of several micro-amps, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised.

Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs.

If the configuration options have enabled the Watchdog Timer internal oscillator LIRC then this will continue to run when in the Sleep Mode and will thus consume some power. For power sensitive applications it may be therefore preferable to use the system clock source for the Watchdog Timer. The LXT, if configured for use, will also consume a limited amount of power, as it continues to run when the device enters the Sleep Mode. To keep the LXT power consumption to a minimum level the LXTLP bit in the CTRL0 register, which controls the low power function, should be set high.

Wake-up

After the system enters the Sleep Mode, it can be woken up from one of various sources listed as follows:

- An external reset
- An external falling edge on PA0 to PA7
- A system interrupt
- A WDT overflow

If the system is woken up by an external reset, the device will experience a full system reset, however, if the device is woken up by a WDT overflow, a Watchdog Timer reset will be initiated. Although both of these wake-up methods will initiate a reset operation, the actual source of the wake-up can be determined by examining the TO and PDF flags. The PDF flag is cleared by a system power-up or executing the clear Watchdog

Timer instructions and is set when executing the "HALT" instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Pins PA0 to PA7 can be setup via the PAWUK register to permit a negative transition on the pin to wake-up the system. When a PA0 to PA7 pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction.

If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke-up the device will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set to "1" before entering the Sleep Mode, then any future interrupt requests will not generate a wake-up function of the related interrupt will be ignored.

No matter what the source of the wake-up event is, once a wake-up event occurs, there will be a time delay before normal program execution resumes. Consult the table for the related time.

| Wake-up Source | Oscillator Type | |
|----------------------------------|-------------------------------------|-------------------------------------|
| | ERC, IRC | Crystal |
| External $\overline{\text{RES}}$ | $t_{\text{RSDT}} + t_{\text{SST1}}$ | $t_{\text{RSDT}} + t_{\text{SST2}}$ |
| PA Port | t_{SST1} | t_{SST2} |
| Interrupt | | |
| WDT Overflow | | |

- Note:
1. t_{RSTD} (reset delay time), t_{SYS} (system clock)
 2. t_{RSTD} is power-on delay, typical time=100ms
 3. $t_{\text{SST1}} = 2$ or $1024 t_{\text{SYS}}$
 4. $t_{\text{SST2}} = 1024 t_{\text{SYS}}$

Wake-up Delay Time

Watchdog Timer

The Watchdog Timer, also known as the WDT, is provided to inhibit program malfunctions caused by the program jumping to unknown locations due to certain uncontrollable external events such as electrical noise.

Watchdog Timer Operation

It operates by providing a device reset when the Watchdog Timer counter overflows. Note that if the Watchdog Timer function is not enabled, then any instructions related to the Watchdog Timer will result in no operation.

Setting up the various Watchdog Timer options are controlled via the configuration options and two internal registers WDTN3 and CTRL1. Enabling the Watchdog Timer can be controlled by both a configuration option and the WDTEN bits in the CTRL1 internal register in the Data Memory.

| Configuration Option | CTRL1 Register | WDT Function |
|----------------------|----------------|--------------|
| Disable | Disable | OFF |
| Disable | Enable | ON |
| Enable | x | ON |

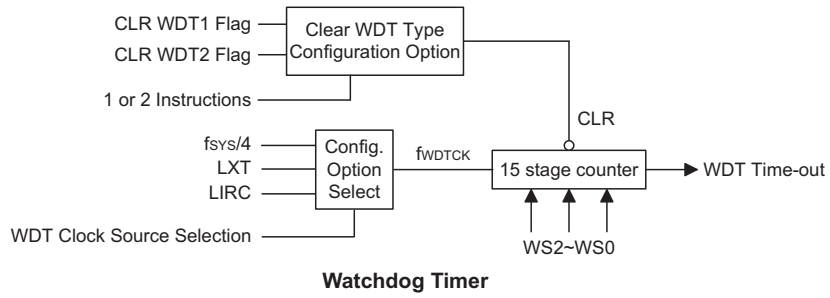
Watchdog Timer On/Off Control

The Watchdog Timer will be disabled if bits WDTEN3~WDTEN0 in the CTRL1 register are written with the binary value 1010B and WDT configuration option is disable. This will be the condition when the device is powered up. Although any other data written to WDTEN3~WDTEN0 will ensure that the Watchdog Timer is enabled, for maximum protection it is recommended that the value 0101B is written to these bits.

The Watchdog Timer clock can emanate from three different sources, selected by configuration option. These are LXT, $f_{SYS}/4$, or LIRC. It is important to note that when the system enters the Sleep Mode the instruction clock is stopped, therefore if the configuration options have selected $f_{SYS}/4$ as the Watchdog Timer clock source, the Watchdog Timer will cease to function. For systems that

operate in noisy environments, using the LIRC or the LXT as the clock source is therefore the recommended choice. The division ratio of the prescaler is determined by bits 0, 1 and 2 of the WDTN3 register, known as WS0, WS1 and WS2. If the Watchdog Timer internal clock source is selected and with the WS0, WS1 and WS2 bits of the WDTN3 register all set high, the prescaler division ratio will be 1:128, which will give a maximum time-out period.

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO. However, if the system is in the Sleep Mode, when a Watchdog Timer time-out occurs, the device will be woken up, the TO bit in the status register will be set and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the Watchdog Timer. The first is an external hardware reset, which means a low level on the external reset pin, the second is using the Clear Watchdog Timer software instructions and the third is when a HALT instruction is executed. There are two methods of using software instructions to clear the Watchdog Timer, one of which must be chosen by configuration option. The first option is to use the single "CLR WDT" instruction while the second is to use the two commands "CLR WDT1" and "CLR WDT2". For the first option, a simple execution of "CLR WDT" will clear the Watchdog Timer while for the second option, both "CLR WDT1" and "CLR WDT2" must both be executed to successfully clear the Watchdog Timer. Note that for this second option, if "CLR WDT1" is used to clear the Watchdog Timer, successive executions of this instruction will have no effect, only the execution of a "CLR WDT2" instruction will clear the Watchdog Timer. Similarly after the "CLR WDT2" instruction has been executed, only a successive "CLR WDT1" instruction can clear the Watchdog Timer.



• **WDTS Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|-----|-----|-----|
| Name | — | — | — | — | — | WS2 | WS1 | WS0 |
| R/W | — | — | — | — | — | R/W | R/W | R/W |
| POR | — | — | — | — | — | 1 | 1 | 1 |

Bit 7~3 : unimplemented, read as "0"

Bit 2~0 **WS2, WS1, WS0**: WDT time-out period selection

- 000: $2^8 t_{WDTCCK}$
- 001: $2^9 t_{WDTCCK}$
- 010: $2^{10} t_{WDTCCK}$
- 011: $2^{11} t_{WDTCCK}$
- 100: $2^{12} t_{WDTCCK}$
- 101: $2^{13} t_{WDTCCK}$
- 110: $2^{14} t_{WDTCCK}$
- 111: $2^{15} t_{WDTCCK}$

Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

In addition to the power-on reset, situations may arise where it is necessary to forcefully apply a reset condition when the microcontroller is running. One example of this is where after power has been applied and the microcontroller is already running, the $\overline{\text{RES}}$ line is forcefully pulled low. In such a case, known as a normal operation reset, some of the microcontroller registers remain unchanged allowing the microcontroller to proceed with normal operation after the reset line is allowed to return high. Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup.

Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset, similar to the $\overline{\text{RES}}$ reset is implemented in situations where the power supply voltage falls below a certain threshold.

Reset Functions

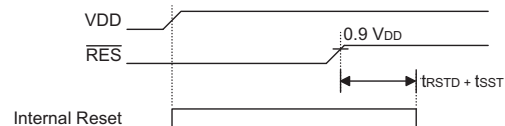
There are five ways in which a microcontroller reset can occur, through events occurring both internally and externally:

- Power-on Reset

The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.

Although the microcontroller has an internal RC reset function, if the VDD power supply rise time is not fast enough or does not stabilise quickly at power-on, the internal reset function may be incapable of providing

proper reset operation. For this reason it is recommended that an external RC network is connected to the $\overline{\text{RES}}$ pin, whose additional time delay will ensure that the $\overline{\text{RES}}$ pin remains low for an extended period to allow the power supply to stabilise. During this time delay, normal operation of the microcontroller will be inhibited. After the $\overline{\text{RES}}$ line reaches a certain voltage value, the reset delay time t_{RSTD} is invoked to provide an extra delay time after which the microcontroller will begin normal operation. The abbreviation SST in the figures stands for System Start-up Timer.

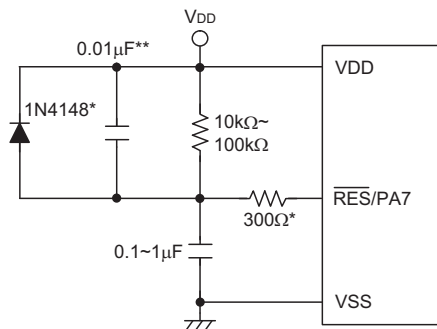


Note: t_{RSTD} is power-on delay, typical time=100ms

Power-On Reset Timing Chart

For most applications a resistor connected between VDD and the $\overline{\text{RES}}$ pin and a capacitor connected between VSS and the $\overline{\text{RES}}$ pin will provide a suitable external reset circuit. Any wiring connected to the $\overline{\text{RES}}$ pin should be kept as short as possible to minimise any stray noise interference.

For applications that operate within an environment where more noise is present the Enhanced Reset Circuit shown is recommended.



Note: "*" It is recommended that this component is added for added ESD protection

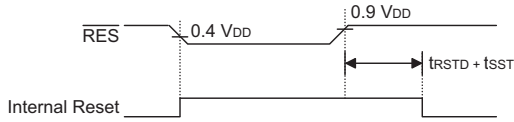
"**" It is recommended that this component is added in environments where power line noise is significant

External $\overline{\text{RES}}$ Circuit

More information regarding external reset circuits is located in Application Note HA0075E on the Holtek website.

• **RES Pin Reset**

This type of reset occurs when the microcontroller is already running and the RES pin is forcefully pulled low by external hardware such as an external switch. In this case as in the case of other reset, the Program Counter will reset to zero and program execution initiated from this point.

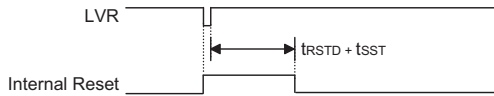


Note: t_{RSTD} is power-on delay, typical time=100ms

RES Reset Timing Chart

• **Low Voltage Reset – LVR**

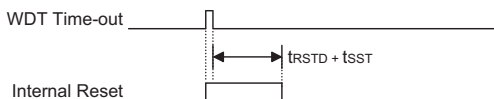
The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device. The LVR function is selected via a configuration option. If the supply voltage of the device drops to within a range of $0.9V \sim V_{LVR}$ such as might occur when changing the battery, the LVR will automatically reset the device internally. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between $0.9V \sim V_{LVR}$ must exist for a time greater than that specified by t_{LVR} in the A.C. characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual V_{LVR} value can be selected via configuration options.



Note: t_{RSTD} is power-on delay, typical time=100ms

Low Voltage Reset Timing Chart

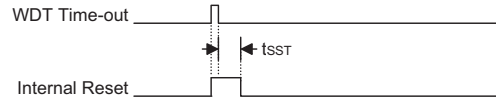
• **Watchdog Time-out Reset during Normal Operation**
The Watchdog time-out Reset during normal operation is the same as a hardware RES pin reset except that the Watchdog time-out flag TO will be set to "1".



Note: t_{RSTD} is power-on delay, typical time=100ms

WDT Time-out Reset during Normal Operation Timing Chart

• **Watchdog Time-out Reset during Sleep mode**
The Watchdog time-out Reset during Sleep mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the A.C. Characteristics for t_{SST} details.



WDT Time-out Reset during Sleep Timing Chart

Note: The t_{SST} can be chosen to be either 1024 or 2 clock cycles via configuration option if the system clock source is provided by ERC or HIRC. The SST is 1024 for HXT or LXT.

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the Sleep function or Watchdog Timer. The reset flags are shown in the table:

| TO | PDF | RESET Conditions |
|----|-----|---------------------------------------------------------|
| 0 | 0 | Power-on reset |
| u | u | RES or LVR reset during Normal or Slow Mode operation |
| 1 | u | WDT time-out reset during Normal or Slow Mode operation |
| 1 | 1 | WDT time-out reset during Sleep Mode operation |

Note: "u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

| Item | Condition After RESET |
|---------------------|--------------------------------------------------|
| Program Counter | Reset to zero |
| Interrupts | All interrupts will be disabled |
| WDT | Clear after reset, WDT begins counting |
| Timer/Event Counter | Timer Counter will be turned off |
| Prescaler | The Timer Counter Prescaler will be cleared |
| Input/Output Ports | I/O ports will be setup as inputs |
| Stack Pointer | Stack Pointer will point to the top of the stack |

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers.

| Register | Power-on Reset | RES or LVR Reset | WDT Time-out (Normal Operation) | WDT Time-out (Sleep) |
|----------|-----------------|------------------|---------------------------------|----------------------|
| PCL | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 |
| MP0 | x x x x x x x x | u u u u u u u u | u u u u u u u u | u u u u u u u u |
| MP1 | x x x x x x x x | u u u u u u u u | u u u u u u u u | u u u u u u u u |
| ACC | x x x x x x x x | u u u u u u u u | u u u u u u u u | u u u u u u u u |
| TBLP | x x x x x x x x | u u u u u u u u | u u u u u u u u | u u u u u u u u |
| TBLH | - x x x x x x x | - u u u u u u u | - u u u u u u u | - u u u u u u u |
| WDS | - - - - - 1 1 1 | - - - - - 1 1 1 | - - - - - 1 1 1 | - - - - - u u u |
| STATUS | - - 0 0 x x x x | - - u u u u u u | - - 1 u u u u u | - - 1 1 u u u u |
| INTC0 | - 0 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - u u u u u u u |
| INTC1 | - - 0 0 - - 0 0 | - - 0 0 - - 0 0 | - - 0 0 - - 0 0 | - - u u - - u u |
| TMR0 | x x x x x x x x | x x x x x x x x | x x x x x x x x | u u u u u u u u |
| TMR0C | 0 0 0 0 1 0 0 0 | 0 0 0 0 1 0 0 0 | 0 0 0 0 1 0 0 0 | u u u u u u u u |
| TMR1 | x x x x x x x x | x x x x x x x x | x x x x x x x x | u u u u u u u u |
| TMR1C | 0 0 0 0 1 - - - | 0 0 0 0 1 - - - | 0 0 0 0 1 - - - | u u u u u - - - |
| PA | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | u u u u u u u u |
| PAC | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | u u u u u u u u |
| PAWK | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | u u u u u u u u |
| PAPU | - 0 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - u u u u u u u |
| PB | - - 1 1 1 1 1 1 | - - 1 1 1 1 1 1 | - - 1 1 1 1 1 1 | - - u u u u u u |
| PBC | - - 1 1 1 1 1 1 | - - 1 1 1 1 1 1 | - - 1 1 1 1 1 1 | - - u u u u u u |
| PBPU | - - 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - 0 0 0 0 0 0 0 | - - u u u u u u |
| PC | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | u u u u u u u u |
| PCC | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | u u u u u u u u |
| PCPU | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | u u u u u u u u |
| CTRL0 | - 0 0 - 0 0 0 0 | - 0 0 - 0 0 0 0 | - 0 0 - 0 0 0 0 | - u u - u u u u |
| CTRL1 | 1 0 0 0 1 0 1 0 | 1 0 0 0 1 0 1 0 | 1 0 0 0 1 0 1 0 | u u u u u u u u |
| SCOMC | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | u u u u u u u u |
| PWM0 | x x x x x x x x | x x x x x x x x | x x x x x x x x | u u u u u u u u |
| ADRL | x x x x - - - - | x x x x - - - - | x x x x - - - - | u u u u - - - - |
| ADRH | x x x x x x x x | x x x x x x x x | x x x x x x x x | u u u u u u u u |
| ADCR | 0 1 0 0 0 0 0 0 | 0 1 0 0 0 0 0 0 | 0 1 0 0 0 0 0 0 | u u u u u u u u |
| ACSR | 1 0 - - - 0 0 0 | 1 0 - - - 0 0 0 | 1 0 - - - 0 0 0 | u u - - - u u u |

Note: "-" not implemented
 "u" means "unchanged"
 "x" means "unknown"

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. Most pins can have either an input or output designation under user program control. Additionally, as there are pull-high resistors and wake-up software configurations, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A,[m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selectable via a register known as PAPU, PBPU and PCPU located in the Data Memory. The pull-high resistors are implemented using weak PMOS transistors. Note that pin PA7 does not have a pull-high resistor selection.

Port A Wake-up

If the HALT instruction is executed, the device will enter the Sleep Mode, where the system clock will stop resulting in power being conserved, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the PA0~PA7 pins from high to low. After a HALT instruction forces the microcontroller into entering the Sleep Mode, the processor will remain or in a low-power state until the logic condition of the selected wake-up pin on Port A changes from high to low. This function is especially suitable for applications that can be woken up via external switches. Note that pins PA0 to PA7 can be selected individually to have this wake-up feature using an internal register known as PAWK, located in the Data Memory.

• PAWK, PAC, PAPU, PBC, PBPU, PCC, PCPU Register

| Register Name | POR | Bit | | | | | | | |
|---------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAWK | 00H | PAWK7 | PAWK6 | PAWK5 | PAWK4 | PAWK3 | PAWK2 | PAWK1 | PAWK0 |
| PAC | FFH | PAC7 | PAC6 | PAC5 | PAC4 | PAC3 | PAC2 | PAC1 | PAC0 |
| PAPU | 00H | — | PAPU6 | PAPU5 | PAPU4 | PAPU3 | PAPU2 | PAPU1 | PAPU0 |
| PBC | 3FH | — | — | PBC5 | PBC4 | PBC3 | PBC2 | PBC1 | PBC0 |
| PBPU | 00H | — | — | PBPU5 | PBPU4 | PBPU3 | PBPU2 | PBPU1 | PBPU0 |
| PCC | FFH | PCC7 | PCC6 | PCC5 | PCC4 | PCC3 | PCC2 | PCC1 | PCC0 |
| PCPU | 00H | PCPU7 | PCPU6 | PCPU5 | PCPU4 | PCPU3 | PCPU2 | PCPU1 | PCPU0 |

"—" Unimplemented, read as "0"

PAWK_n: PA wake-up function enable

0: disable

1: enable

PAC_n/PBC_n/PCC_n: I/O type selection

0: output

1: input

PAPU_n/PBPU_n/PCPU_n: Pull-high function enable

0: disable

1: enable

I/O Port Control Registers

Each Port has its own control register, known as PAC, PBC, PCC which controls the input/output configuration. With this control register, each I/O pin with or without pull-high resistors can be reconfigured dynamically under software control. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

Pin-shared Functions

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers but by supplying pins with multi-functions, many of these difficulties can be overcome. For some pins, the chosen function of the multi-function I/O pins is set by configuration options while for others the function is set by application program control.

- **External Interrupt Input**
The external interrupt pin, INT, is pin-shared with an I/O pin. To use the pin as an external interrupt input the correct bits in the INTC0 register must be programmed. The pin must also be setup as an input by setting the PAC3 bit in the Port Control Register. A pull-high resistor can also be selected via the appropriate port pull-high resistor register. Note that even if the pin is setup as an external interrupt input the I/O function still remains.
- **External Timer/Event Counter Input**
The Timer/Event Counter pins, TC0 is pin-shared with I/O pins. For these shared pins to be used as Timer/Event Counter inputs, the Timer/Event Counter must be configured to be in the Event Counter or Pulse Width Capture Mode. This is achieved by setting the appropriate bits in the Timer/Event Counter Control Register. The pins must also be setup as inputs by setting the appropriate bit in the Port Control Register. Pull-high resistor options can also be selected using the port pull-high resistor registers. Note that even if the pin is setup as an external timer input the I/O function still remains.

- **PFD Output**
The PFD function output is pin-shared with an I/O pin. The output function of this pin is chosen using the CTRL0 register. Note that the corresponding bit of the port control register, must setup the pin as an output to enable the PFD output. If the port control register has setup the pin as an input, then the pin will function as a normal logic input with the usual pull-high selection, even if the PFD function has been selected.
- **PWM Outputs**
The PWM function whose outputs are pin-shared with I/O pins. The PWM output functions are chosen using the CTRL0 registers. Note that the corresponding bit of the port control registers, for the output pin, must setup the pin as an output to enable the PWM output. If the pins are setup as inputs, then the pin will function as a normal logic input with the usual pull-high selections, even if the PWM registers have enabled the PWM function.
- **SCOM Driver Pins**
Pins PB0~PB3 on Port B can be used as LCD COM driver pins. This function is controlled using the SCOMC register which will generate the necessary 1/2 bias signals on these four pins.
- **A/D Inputs**
Each device in this series has either four or eight inputs to the A/D converter. All of these analog inputs are pin-shared with I/O pins. If these pins are to be used as A/D inputs and not as I/O pins then the corresponding PCRn bits in the A/D converter control register, ADCR, must be properly setup. There are no configuration options associated with the A/D converter. If chosen as I/O pins, then full pull-high resistor configuration options remain, however if used as A/D inputs then any pull-high resistor configuration options associated with these pins will be automatically disconnected.

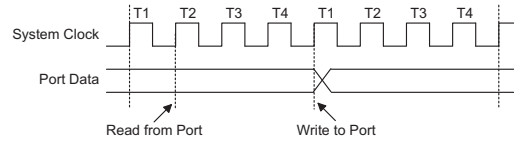
I/O Pin Structures

The diagrams illustrate the I/O pin internal structures. As the exact logical construction of the I/O pin may differ from these drawings, they are supplied as a guide only to assist with the functional understanding of the I/O pins.

Programming Considerations

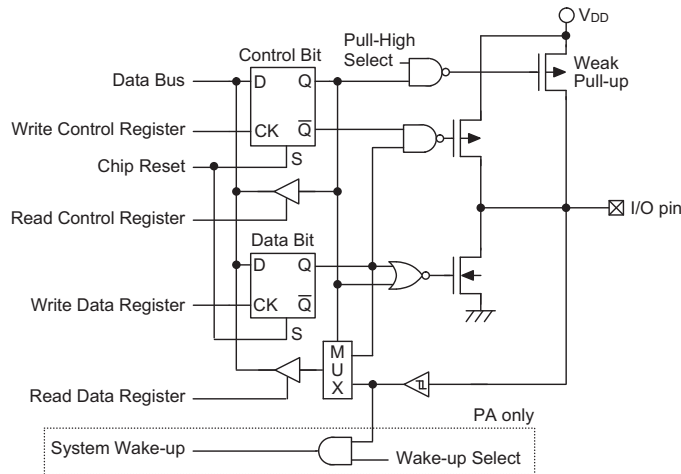
Within the user program, one of the first things to consider is port initialisation. After a reset, the I/O data register and I/O port control register will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high options have been selected. If the port control registers, are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data register is first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct value into the port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire

port, modify it to the required new bit values and then re-write this data back to the output ports.

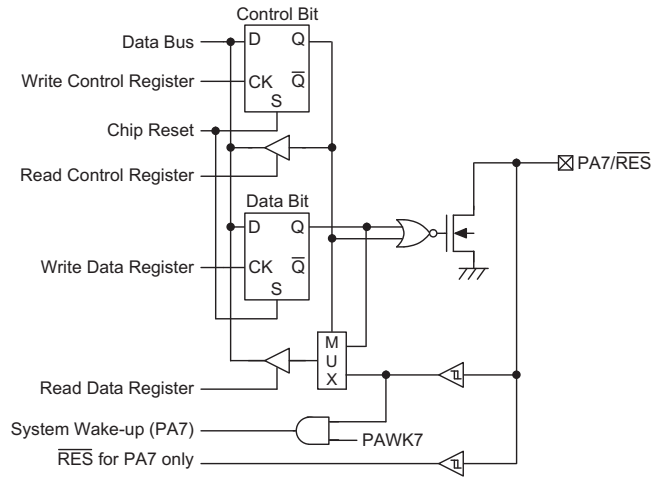


Read Modify Write Timing

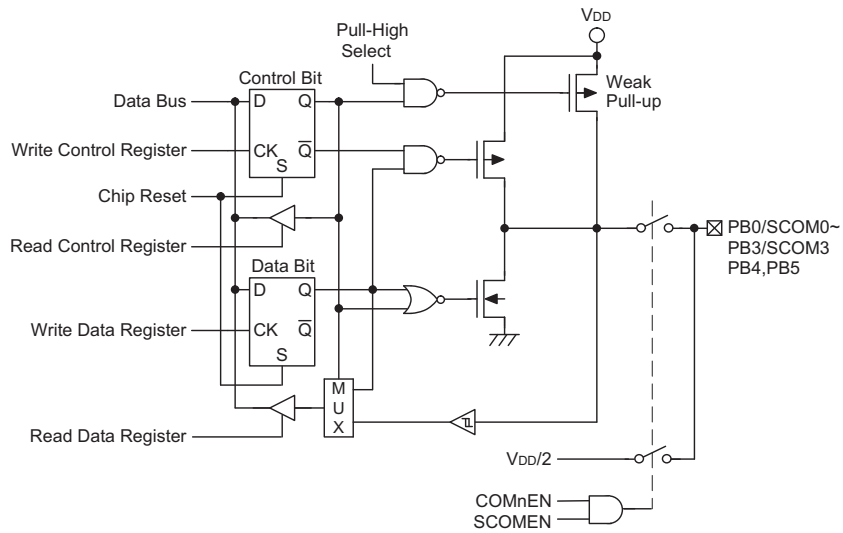
Pins PA0 to PA7 each have a wake-up functions, selected via the PAWK register. When the device is in the Sleep Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the these pins. Single or multiple pins on Port A can be setup to have this function.



Generic Input/Output Ports



PA7 NMOS Input/Output Port



PB Input/Output Port

VFD Driver

The device includes a VFD driver function to drive VFD panel high voltage filaments and buzzer. The microcontroller communicates serially with the VFD driver transmitting the display data into a 24-bit shift register within the driver. This VFD driver converts the shift register into VFD panel driving signals and makes the necessary voltage level shifting. The microcontroller will only transmit data to the VFD driver, no data is transmitted from the VFD driver to the microcontroller.

VFD Interface

A five line interface exists between the microcontroller and the VFD driver as shown in the diagram.

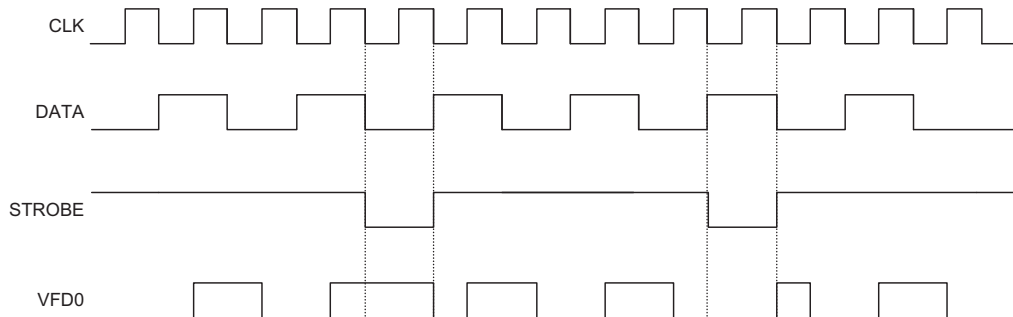
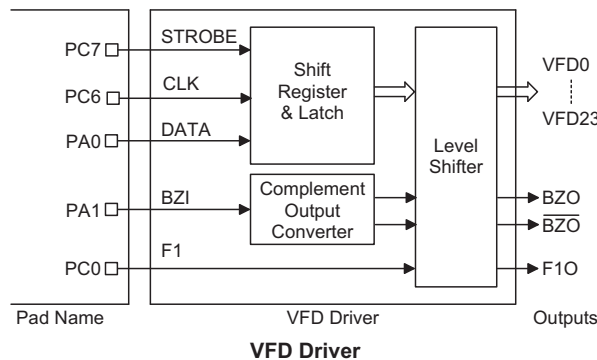
Data transmission between the microcontroller and the VFD interface is conducted via a three line interface using the CLK, DATA and STROBE lines. As data communication is only one way the microcontroller I/O pins must be setup as outputs.

The buzzer control input BZI will be transformed into a complementary pair of outputs BZO and \overline{BZO} by a converter in the VFD driver. These complementary buzzer outputs will also be level shifted to a higher voltage by the converter. The VFD driver filament control input, F1, will also be shifted to a high voltage output called F1O, that can be used to switch the filaments on and off.

24-bit Shift Register/Latch

Data transmitted from the microcontroller is transmitted serially and will be first written into a 24-bit shift register located within the VFD driver. These 24-bits are used to control the VFD panel segments, VFD0~VFD15, and grid, VFD16~VFD23, lines. The control method is as follows:

- Use the "DATA" and "CLK" lines to shift data into the internal 24-bit shift register. Data is clocked into the shift-register on the positive clock edge. This data corresponds to the desired VFD0~VFD23 output display data. The VFD outputs will only change if the STROBE line is high. If the STROBE line is low, only the shift register data will be modified and the VFD outputs will remain the same.
- Use the "STROBE" line to latch the shift-register data to the VFD0~VFD23 outputs. When the STROBE line is high, the shift register data will be latched to the VFD lines. Note that the STROBE line is level and not edge triggered.



VFD Display Control Timing Diagram

The accompanying table shows the 24-bit shift register/latch function truth table:

| Clock | Strobe | Data | VFD0 | VFDn |
|-------|--------|------|-----------|-----------|
| ↑ | 0 | X | No change | No change |
| ↑ | 1 | 0 | 0 | VFDn-1 |
| ↑ | 1 | 1 | 1 | VFDn-1 |
| ↓ | 1 | 1 | No change | No change |

Note: "X" means don't care
 "VFDn" means VFD1~VFD23

Programming Considerations

After power on all the I/O lines will be automatically setup as inputs. However as lines PB2~PB5 are used to drive the VFD interface, they should be setup as outputs after power is applied to the device. Allowing the VFD interface control lines to be setup as inputs will create an incorrect VFD display operation. It is advised that the configuration options select pull-high resistors to be connected to these lines to keep the lines at a fixed high level when power is initially applied and until the lines can be setup as outputs.

Programming Example

The following example shows how the VFD display data is programmed by the microcontroller.

```

; It's necessary to define strobe/clk/data for related I/O port.
Data_2_register:          ; send data to vfd driver
    mov     a,024d        ; shift register counter
    mov     count,a
    clr     strobe        ; strobe = 0
data_2_register_1:
    clr     clk            ; clk = 0
    set     data           ; data = 1
    snz     vfd_grid.7
    clr     data           ; data = 0
    rlc     vfd_seg1       ; shift data to vfd[7:0]
    rlc     vfd_seg2       ; shift data to vfd[15:8]
    rlc     vfd_grid       ; shift data to vfd[22:16]
    set     clk            ; clk = 1 (rising edge)
    sdz     count
    jmp     data_2_register_1
    set     strobe         ; strobe = 1, vfd output
    ret
  
```

Timer/Event Counters

The provision of timers form an important part of any microcontroller, giving the designer a means of carrying out time related functions. The devices contain from one to three count-up timer of 8-bit capacity. As the timers have three different operating modes, they can be configured to operate as a general timer, an external event counter or as a pulse width capture device. The provision of an internal prescaler to the clock circuitry on gives added range to the timers.

There are two types of registers related to the Timer/Event Counters. The first is the register that contains the actual value of the timer and into which an initial value can be preloaded. Reading from this register retrieves the contents of the Timer/Event Counter. The second type of associated register is the Timer Control Register which defines the timer options and determines how the timer is to be used. The device can have the timer clock configured to come from the internal clock source. In addition, the timer clock source can also be configured to come from an external timer pin.

Configuring the Timer/Event Counter Input Clock Source

The Timer/Event Counter clock source can originate from various sources, an internal clock or an external pin. The internal clock source is used when the timer is in the timer mode or in the pulse width capture mode. For some Timer/Event Counters, this internal clock source is first divided by a prescaler, the division ratio of which is conditioned by the Timer Control Register bits T0PSC0~T0PSC2. For Timer/Event Counter 0, the internal clock source can be either f_{SYS} or the LXT Oscillator, the choice of which is determined by the T0S bit in the TMR0C register.

An external clock source is used when the timer is in the event counting mode, the clock source being provided on an external timer pin TCn. Depending upon the condition of the TnEG bit, each high to low, or low to high transition on the external timer pin will increment the counter by one.

Timer Registers – TMR0, TMR1

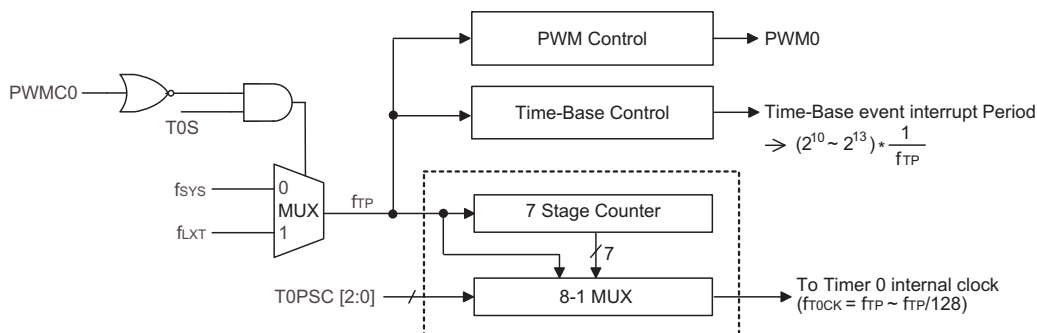
The timer registers are special function registers located in the Special Purpose Data Memory and is the place where the actual timer value is stored. These registers are known as TMR0 and TMR1. The value in the timer registers increases by one each time an internal clock pulse is received or an external transition occurs on the external timer pin. The timer will count from the initial value loaded by the preload register to the full count of FFH at which point the timer overflows and an internal interrupt signal is generated. The timer value will then be reset with the initial preload register value and continue counting.

Note that to achieve a maximum full range count of FFH, the preload register must first be cleared to all zeros. It should be noted that after power-on, the preload registers will be in an unknown condition. Note that if the Timer/Event Counter is in an OFF condition and data is written to its preload register, this data will be immediately written into the actual counter. However, if the counter is enabled and counting, any new data written into the preload data register during this period will remain in the preload register and will only be written into the actual counter the next time an overflow occurs.

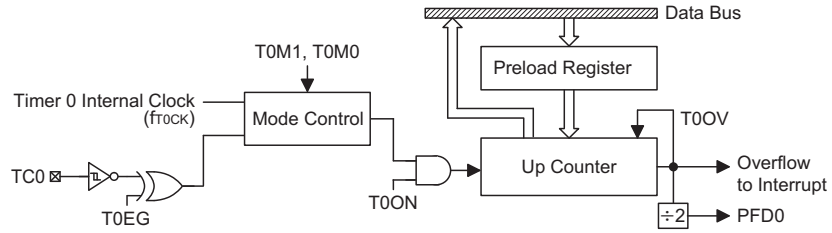
Timer Control Registers – TMR0C, TMR1C

The flexible features of the Holtek microcontroller Timer/Event Counters enable them to operate in three different modes, the options of which are determined by the contents of their respective control register.

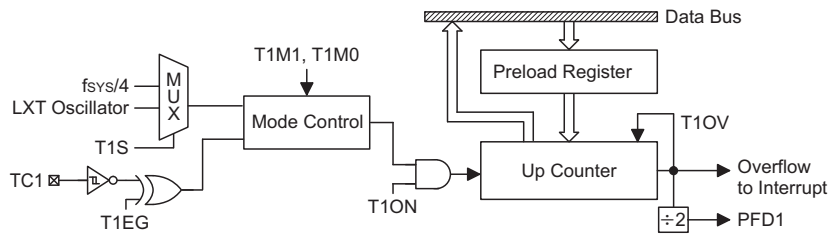
The Timer Control Register is known as TMRnC. It is the Timer Control Register together with its corresponding timer register that control the full operation of the Timer/Event Counter. Before the timer can be used, it is essential that the Timer Control Register is fully programmed with the right data to ensure its correct operation, a process that is normally carried out during program initialisation.



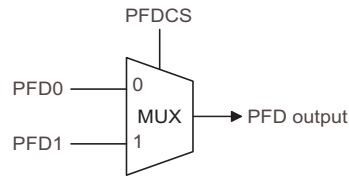
Clock Structure for Timer/PWM/Time Base



8-bit Timer/Event Counter 0 Structure



8-bit Timer/Event Counter 1 Structure



Note: If PWM0 is enabled, then f_{TP} comes from f_{SYS} (ignore T0S)

• TMR0C Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|-----|------|------|--------|--------|--------|
| Name | T0M1 | T0M0 | T0S | T0ON | T0EG | T0PSC2 | T0PSC1 | T0PSC0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

- Bit 7,6 **T0M1, T0M0:** Timer0 operation mode selection
 00: no mode available
 01: event counter mode
 10: timer mode
 11: pulse width capture mode
- Bit 5 **T0S:** timer clock source
 0: f_{SYS}
 1: LXT oscillator
 T0S selects the clock source for f_{TP} which is provided for Timer 0, Timer 2, the Time-Base and the PWM. If the PWM is enabled, then f_{SYS} will be selected, overriding the T0S selection.
- Bit 4 **T0ON:** Timer/event counter counting enable
 0: disable
 1: enable
- Bit 3 **T0EG:**
 Event counter active edge selection
 0: count on raising edge
 1: count on falling edge
 Pulse Width Capture active edge selection
 0: start counting on falling edge, stop on raising edge
 1: start counting on raising edge, stop on falling edge
- Bit 2~0 **T0PSC2, T0PSC1, T0PSC0:** Timer prescaler rate selection
 Timer internal clock=
 000: f_{TP}
 001: $f_{TP}/2$
 010: $f_{TP}/4$
 011: $f_{TP}/8$
 100: $f_{TP}/16$
 101: $f_{TP}/32$
 110: $f_{TP}/64$
 111: $f_{TP}/128$

• TMR1C Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|-----|------|------|---|---|---|
| Name | T1M1 | T1M0 | T1S | T1ON | T1EG | — | — | — |
| R/W | R/W | R/W | R/W | R/W | R/W | — | — | — |
| POR | 0 | 0 | 0 | 0 | 1 | — | — | — |

- Bit 7,6 **T1M1, T1M0:** Timer 1 Operation mode selection
 00: no mode available
 01: event counter mode
 10: timer mode
 11: pulse width capture mode
- Bit 5 **T1S:** timer clock source
 0: $f_{SYS}/4$
 1: LXT oscillator
- Bit 4 **T1ON:** Timer/event counter counting enable
 0: disable
 1: enable
- Bit 3 **T1EG:**
 Event counter active edge selection
 0: count on raising edge
 1: count on falling edge
 Pulse Width Capture active edge selection
 0: start counting on falling edge, stop on raising edge
 1: start counting on raising edge, stop on falling edge
- Bit 2~0 unimplemented, read as "0"

To choose which of the three modes the timer is to operate in, either in the timer mode, the event counting mode or the pulse width capture mode, bits 7 and 6 of the Timer Control Register, which are known as the bit pair TnM1/TnM0, must be set to the required logic levels. The timer-on bit, which is bit 4 of the Timer Control Register and known as TnON, provides the basic on/off control of the respective timer. Setting the bit high allows the counter to run, clearing the bit stops the counter. Bits 0~2 of the Timer Control Register determine the division ratio of the input clock prescaler. The prescaler bit settings have no effect if an external clock source is used. If the timer is in the event count or pulse width capture mode, the active transition edge level type is selected by the logic level of bit 3 of the Timer Control Register which is known as TnEG. The TnS bit selects the internal clock source if used.

Timer Mode

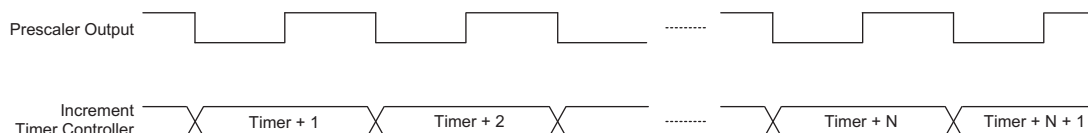
In this mode, the Timer/Event Counter can be utilised to measure fixed time intervals, providing an internal interrupt signal each time the Timer/Event Counter overflows. To operate in this mode, the Operating Mode

Select bit pair, TnM1/TnM0, in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode
 Select Bits for the Timer Mode

| Bit7 | Bit6 |
|------|------|
| 1 | 0 |

In this mode the internal clock is used as the timer clock. The timer input clock source is either f_{SYS} , $f_{SYS}/4$ or the LXT oscillator. However, this timer clock source is further divided by a prescaler, the value of which is determined by the bits TnPSC2~TnPSC0 in the Timer Control Register. The timer-on bit, TnON must be set high to enable the timer to run. Each time an internal clock high to low transition occurs, the timer increments by one; when the timer is full and overflows, an interrupt signal is generated and the timer will reload the value already loaded into the preload register and continue counting. A timer overflow condition and corresponding internal interrupt is one of the wake-up sources, however, the internal interrupts can be disabled by ensuring that the ETnI bits of the INTCn register are reset to zero.


Timer Mode Timing Chart

Event Counter Mode

In this mode, a number of externally changing logic events, occurring on the external timer TCn pin, can be recorded by the Timer/Event Counter. To operate in this mode, the Operating Mode Select bit pair, TnM1/TnM0, in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Event Counter Mode

| Bit7 | Bit6 |
|------|------|
| 0 | 1 |

In this mode, the external timer TCn pin, is used as the Timer/Event Counter clock source, however it is not divided by the internal prescaler. After the other bits in the Timer Control Register have been setup, the enable bit TnON, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter to run. If the Active Edge Select bit, TnEG, which is bit 3 of the Timer Control Register, is low, the Timer/Event Counter will increment each time the external timer pin receives a low to high transition. If the TnEG is high, the counter will increment each time the external timer pin receives a high to low transition. When it is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the corresponding Interrupt Control Register, is reset to zero.

As the external timer pin is shared with an I/O pin, to ensure that the pin is configured to operate as an event counter input pin, two things have to happen. The first is to ensure that the Operating Mode Select bits in the

Timer Control Register place the Timer/Event Counter in the Event Counting Mode, the second is to ensure that the port control register configures the pin as an input. It should be noted that in the event counting mode, even if the microcontroller is in the Sleep Mode, the Timer/Event Counter will continue to record externally changing logic events on the timer input TCn pin. As a result when the timer overflows it will generate a timer interrupt and corresponding wake-up source.

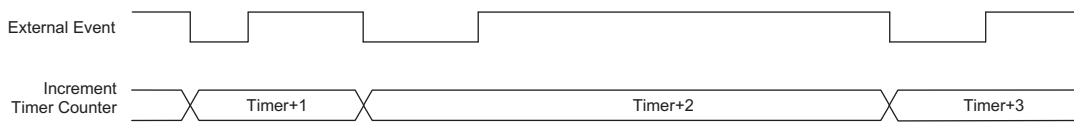
Pulse Width Capture Mode

In this mode, the Timer/Event Counter can be utilised to measure the width of external pulses applied to the external timer pin. To operate in this mode, the Operating Mode Select bit pair, TnM1/TnM0, in the Timer Control Register must be set to the correct value as shown.

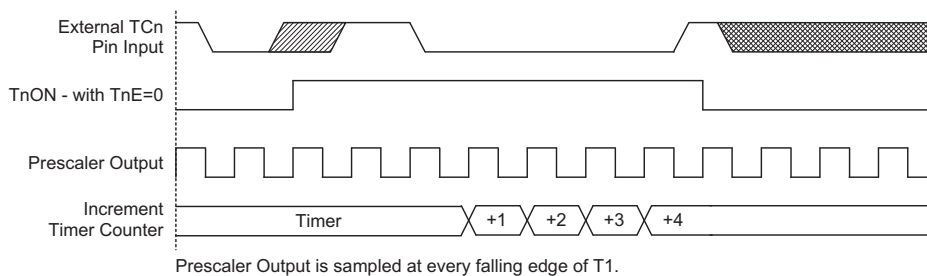
Control Register Operating Mode Select Bits for the Pulse Width Capture Mode

| Bit7 | Bit6 |
|------|------|
| 1 | 1 |

In this mode the internal clock, f_{SYS} , $f_{SYS}/4$ or the LXT, is used as the internal clock for the 8-bit Timer/Event Counter. However, the clock source, f_{SYS} , for the 8-bit timer is further divided by a prescaler, the value of which is determined by the Prescaler Rate Select bits TnPSC2~TnPSC0, which are bits 2~0 in the Timer Control Register. After the other bits in the Timer Control Register have been setup, the enable bit TnON, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter, however it will not actually start counting until an active edge is received on the external timer pin.



Event Counter Mode Timing Chart (TnEG=1)



Pulse Width Capture Mode Timing Chart (TnE=0)

If the Active Edge Select bit TnEG, which is bit 3 of the Timer Control Register, is low, once a high to low transition has been received on the external timer pin, the Timer/Event Counter will start counting until the external timer pin returns to its original high level. At this point the enable bit will be automatically reset to zero and the Timer/Event Counter will stop counting. If the Active Edge Select bit is high, the Timer/Event Counter will begin counting once a low to high transition has been received on the external timer pin and stop counting when the external timer pin returns to its original low level. As before, the enable bit will be automatically reset to zero and the Timer/Event Counter will stop counting. It is important to note that in the pulse width capture Mode, the enable bit is automatically reset to zero when the external control signal on the external timer pin returns to its original level, whereas in the other two modes the enable bit can only be reset to zero under program control.

The residual value in the Timer/Event Counter, which can now be read by the program, therefore represents the length of the pulse received on the TCn pin. As the enable bit has now been reset, any further transitions on the external timer pin will be ignored. The timer cannot begin further pulse width capture until the enable bit is set high again by the program. In this way, single shot pulse measurements can be easily made.

It should be noted that in this mode the Timer/Event Counter is controlled by logical transitions on the external timer pin and not by the logic level. When the Timer/Event Counter is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the corresponding Interrupt Control Register, is reset to zero.

As the TCn pin is shared with an I/O pin, to ensure that the pin is configured to operate as a pulse width capture pin, two things have to happen. The first is to ensure that the Operating Mode Select bits in the Timer Control Register place the Timer/Event Counter in the pulse width capture Mode, the second is to ensure that the port control register configures the pin as an input.

Prescaler

Bits TnPSC0~TnPSC2 of the TMRnC register can be used to define a division ratio for the internal clock source of the Timer/Event Counter enabling longer time out periods to be setup.

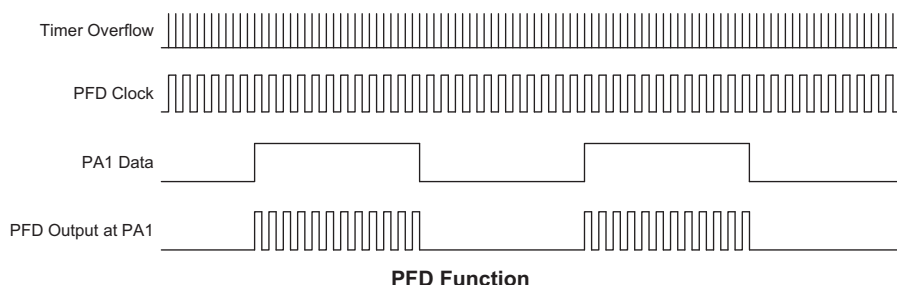
PFD Function

The Programmable Frequency Divider provides a means of producing a variable frequency output suitable for applications, such as piezo-buzzer driving or other interfaces requiring a precise frequency generator.

The Timer/Event Counter overflow signal is the clock source for the PFD function, which is controlled by PFDCS bit in CTRL0. For applicable devices the clock source can come from either Timer/Event Counter 0 or Timer/Event Counter 1. The output frequency is controlled by loading the required values into the timer prescaler and timer registers to give the required division ratio. The counter will begin to count-up from this preload register value until full, at which point an overflow signal is generated, causing both the PFD outputs to change state. The counter will then be automatically reloaded with the preload register value and continue counting-up.

If the CTRL0 register has selected the PFD function, then for PFD output to operate, it is essential for the Port A control register PAC, to setup the PFD pins as outputs. PA1 must be set high to activate the PFD. The output data bits can be used as the on/off control bit for the PFD outputs. Note that the PFD outputs will all be low if the output data bit is cleared to zero.

Using this method of frequency generation, and if a crystal oscillator is used for the system clock, very precise values of frequency can be generated.



I/O Interfacing

The Timer/Event Counter, when configured to run in the event counter or pulse width capture mode, requires the use of an external timer pin for its operation. As this pin is a shared pin it must be configured correctly to ensure that it is setup for use as a Timer/Event Counter input pin. This is achieved by ensuring that the mode select bits in the Timer/Event Counter control register, select either the event counter or pulse width capture mode. Additionally the corresponding Port Control Register bit must be set high to ensure that the pin is setup as an input. Any pull-high resistor connected to this pin will remain valid even if the pin is used as a Timer/Event Counter input.

Programming Considerations

When configured to run in the timer mode, the internal system clock is used as the timer clock source and is therefore synchronised with the overall operation of the microcontroller. In this mode when the appropriate timer register is full, the microcontroller will generate an internal interrupt signal directing the program flow to the respective internal interrupt vector. For the pulse width capture mode, the internal system clock is also used as the timer clock source but the timer will only run when the correct logic condition appears on the external timer input pin. As this is an external event and not synchronised with the internal timer clock, the microcontroller will only see this external event when the next timer clock pulse arrives. As a result, there may be small differences in measured values requiring programmers to take this into account during programming. The same applies if the timer is configured to be in the event counting mode, which again is an external event and not synchronised with the internal system or timer clock.

When the Timer/Event Counter is read, or if data is written to the preload register, the clock is inhibited to avoid errors, however as this may result in a counting error, this should be taken into account by the programmer. Care must be taken to ensure that the timers are properly initialised before using them for the first time. The associated timer enable bits in the interrupt control register must be properly set otherwise the internal interrupt associated with the timer will remain inactive. The edge select, timer mode and clock source control bits in timer control register must also be correctly set to ensure the timer is properly configured for the required application. It is also important to ensure that an initial value is first loaded into the timer registers before the timer is switched on; this is because after power-on the initial values of the timer registers are unknown. After the timer has been initialised the timer can be turned on and off by controlling the enable bit in the timer control register.

When the Timer/Event Counter overflows, its corresponding interrupt request flag in the interrupt control register will be set. If the Timer/Event Counter interrupt is enabled this will in turn generate an interrupt signal. However irrespective of whether the interrupts are enabled or not, a Timer/Event Counter overflow will also generate a wake-up signal if the device is in a Power-down condition. This situation may occur if the Timer/Event Counter is in the Event Counting Mode and if the external signal continues to change state. In such a case, the Timer/Event Counter will continue to count these external events and if an overflow occurs the device will be woken up from its Power-down condition. To prevent such a wake-up from occurring, the timer interrupt request flag should first be set high before issuing the "HALT" instruction to enter the Sleep Mode.

Timer Program Example

The program shows how the Timer/Event Counter registers are setup along with how the interrupts are enabled and managed. Note how the Timer/Event Counter is turned on, by setting bit 4 of the Timer Control Register. The Timer/Event Counter can be turned off in a similar way by clearing the same bit. This example program sets the Timer/Event Counters to be in the timer mode, which uses the internal system clock as their clock source.

Time Base

The device includes a Time Base function which is used to generate a regular time interval signal.

The Time Base time interval magnitude is determined using an internal 13 stage counter sets the division ratio of the clock source. This division ratio is controlled by both the TBSEL0 and TBSEL1 bits in the CTRL1 register. The clock source is selected using the T0S bit in the TMR0C register.

When the Time Base time out, a Time Base interrupt signal will be generated. It should be noted that as the Time Base clock source is the same as the Timer/Event Counter clock source, care should be taken when programming.

• PFD Programming Example

```

org 04h          ; external interrupt vector

org 08h          ; Timer Counter 0 interrupt vector
jmp tmr0int      ; jump here when Timer 0 overflows
:               :
org 20h          ; main program
:               :
;internal Timer 0 interrupt routine
tmr0int:
:
; Timer 0 main program placed here
:
:
begin:
;setup Timer 0 registers
mov a,09bh      ; setup Timer 0 preload value
mov tmr0,a
mov a,081h      ; setup Timer 0 control register
mov tmr0c,a     ; timer mode and prescaler set to /2
;setup interrupt register
mov a,00dh      ; enable master interrupt and both timer interrupts
mov intc0,a
:               :
set tmr0c.4     ; start Timer 0
:               :

```

Pulse Width Modulator

Every device includes a multiple output 8-bit PWM function. Useful for such applications such as motor speed control, the PWM function provides outputs with a fixed frequency but with a duty cycle that can be varied by setting particular values into the corresponding PWM register.

PWM Operation

A single register, known as PWMn and located in the Data Memory is assigned to each Pulse Width Modulator channel. It is here that the 8-bit value, which represents the overall duty cycle of one modulation cycle of the output waveform, should be placed. To increase the PWM modulation frequency, each modulation cycle is subdivided into two or four individual modulation subsections, known as the 7+1 mode or 6+2 mode respectively. The required mode and the on/off control for each PWM channel is selected using the CTRL0 register. Note that when using the PWM, it is only necessary to write the required value into the PWMn register and select the required mode setup and on/off control using the CTRL0 registers, the subdivision of the waveform into its sub-modulation cycles is implemented automatically within the microcontroller hardware. The PWM clock source is the system clock f_{SYS} . This method of dividing the original modulation cycle into a further 2 or 4 sub-cycles enable the generation of higher PWM frequencies which allow a wider range of applications to be served. The difference between what is known as the PWM cycle frequency and the PWM modulation frequency should be understood. As the PWM clock is the system clock, f_{SYS} , and as the PWM value is 8-bits wide, the overall PWM cycle frequency is $f_{SYS}/256$. However, when in the 7+1 mode of operation the PWM modulation frequency will be $f_{SYS}/128$, while the PWM modulation frequency for the 6+2 mode of operation will be $f_{SYS}/64$.

| PWM Modulation | PWM Cycle Frequency | PWM Cycle Duty |
|-----------------------------------------------------------------------|---------------------|----------------|
| $f_{SYS}/64$ for (6+2) bits mode $f_{SYS}/128$ for (7+1) bits mode | $f_{SYS}/256$ | $[PWM]/256$ |

6+2 PWM Mode

Each full PWM cycle, as it is controlled by an 8-bit PWM register, has 256 clock periods. However, in the 6+2 PWM mode, each PWM cycle is subdivided into four individual sub-cycles known as modulation cycle 0 ~ modulation cycle 3, denoted as i in the table. Each one of these four sub-cycles contains 64 clock cycles. In this mode, a modulation frequency increase of four is achieved. The 8-bit PWM register value, which represents the overall duty cycle of the PWM waveform, is di-

vided into two groups. The first group which consists of bit2~bit7 is denoted here as the DC value. The second group which consists of bit0~bit1 is known as the AC value. In the 6+2 PWM mode, the duty cycle value of each of the four modulation sub-cycles is shown in the following table.

| Parameter | AC (0~3) | DC (Duty Cycle) |
|----------------------------------------|-------------|-------------------|
| Modulation cycle i ($i=0\sim3$) | $i < AC$ | $\frac{DC+1}{64}$ |
| | $i \geq AC$ | $\frac{DC}{64}$ |

6+2 Mode Modulation Cycle Values

The following diagram illustrates the waveforms associated with the 6+2 mode of PWM operation. It is important to note how the single PWM cycle is subdivided into 4 individual modulation cycles, numbered from 0~3 and how the AC value is related to the PWM value.

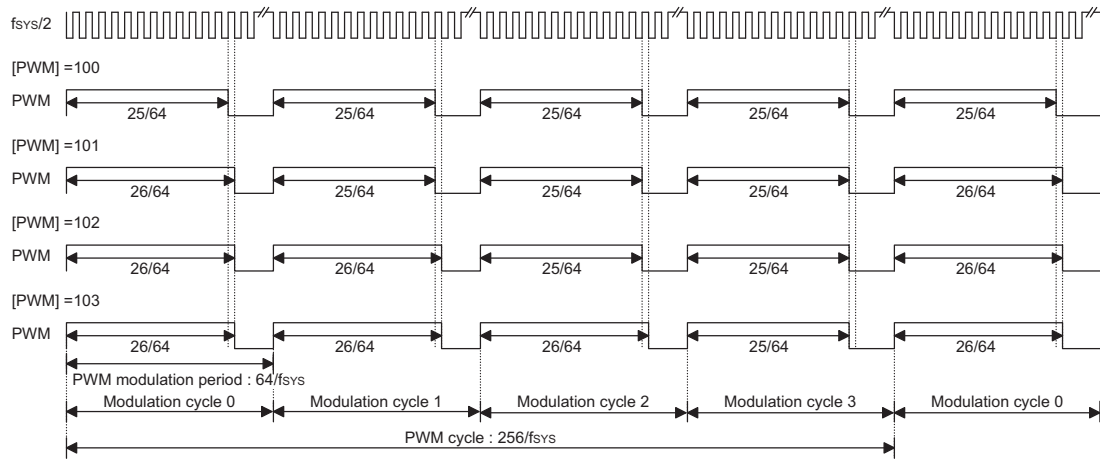
7+1 PWM Mode

Each full PWM cycle, as it is controlled by an 8-bit PWM register, has 256 clock periods. However, in the 7+1 PWM mode, each PWM cycle is subdivided into two individual sub-cycles known as modulation cycle 0 ~ modulation cycle 1, denoted as i in the table. Each one of these two sub-cycles contains 128 clock cycles. In this mode, a modulation frequency increase of two is achieved. The 8-bit PWM register value, which represents the overall duty cycle of the PWM waveform, is divided into two groups. The first group which consists of bit1~bit7 is denoted here as the DC value. The second group which consists of bit0 is known as the AC value. In the 7+1 PWM mode, the duty cycle value of each of the two modulation sub-cycles is shown in the following table.

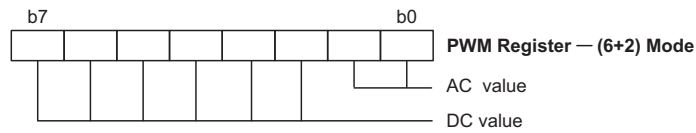
| Parameter | AC (0~1) | DC (Duty Cycle) |
|----------------------------------------|-------------|--------------------|
| Modulation cycle i ($i=0\sim1$) | $i < AC$ | $\frac{DC+1}{128}$ |
| | $i \geq AC$ | $\frac{DC}{128}$ |

7+1 Mode Modulation Cycle Values

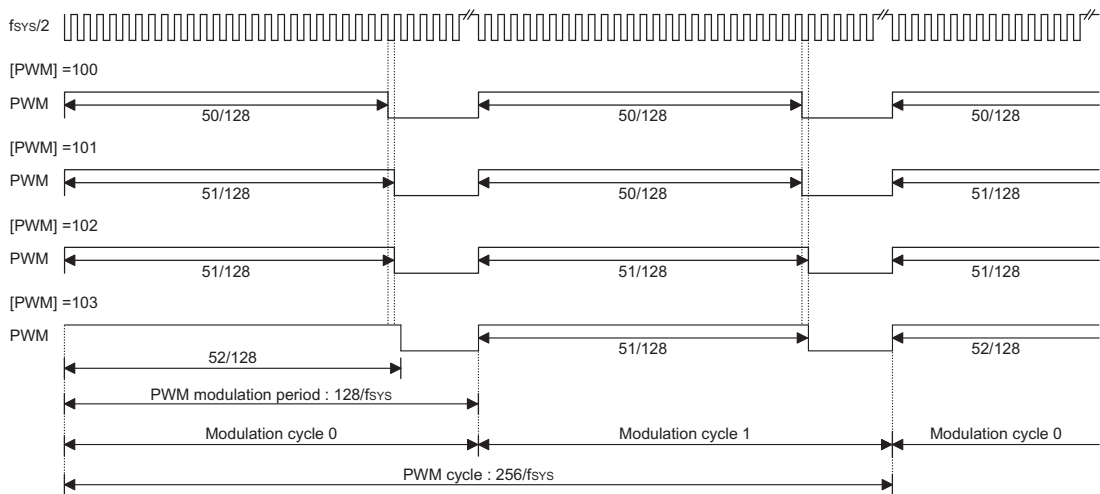
The following diagram illustrates the waveforms associated with the 7+1 mode PWM operation. It is important to note how the single PWM cycle is subdivided into 2 individual modulation cycles, numbered 0 and 1 and how the AC value is related to the PWM value.



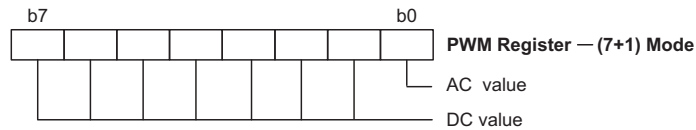
6+2 PWM Mode



PWM Register for 6+2 Mode



7+1 PWM Mode



PWM Register for 7+1 Mode

PWM Output Control

The PWM outputs is pin-shared with the I/O pins PA4. To operate as a PWM output and not as an I/O pin, the correct bits must be set in the CTRL0 register. A zero value must also be written to the corresponding bit in the I/O port control register PAC.4 to ensure that the corresponding PWM output pin is setup as an output. After these two initial steps have been carried out, and of course after the required PWM value has been written into the PWMn register, writing a high value to the corresponding bit in the output data register PA.4 will enable

the PWM data to appear on the pin. Writing a zero value will disable the PWM output function and force the output low. In this way, the Port data output registers can be used as an on/off control for the PWM function. Note that if the CTRL0 registers have selected the PWM function, but a high value has been written to its corresponding bit in the PAC control register to configure the pin as an input, then the pin can still function as a normal input line, with pull-high resistor options.

• PWM Programming Example

The following sample program shows how the PWM0 output is setup and controlled.

```
mov a, 64h           ; setup PWM value of decimal 100
mov pwm0, a
set ctrl0.5         ; select the 7+1 PWM mode
set ctrl0.3         ; select pin PA4 to have a PWM function
clr pac.4           ; setup pin PA4 as an output
set pa.4            ; enable the PWM output
::
clr pa.4            ; disable the PWM output_pin
                   ; PA4 forced low
```

Analog to Digital Converter

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Overview

The device contains an 4/8-channel analog to digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into either a 12-bit digital value.

The accompanying block diagram shows the overall internal structure of the A/D converter, together with its associated registers.

A/D Converter Data Registers – ADRL, ADRH

The device, which has an internal 12-bit A/D converter, requires two data registers, a high byte register, known as ADRH, and a low byte register, known as ADRL. After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value. Only the high byte register, ADRH, utilises its full 8-bit contents. The low byte register utilises only 4 bit of its 8-bit contents as it contains only the lowest bits of the 12-bit converted value.

In the following table, D0~D11 is the A/D conversion data result bits.

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| ADRL | D3 | D2 | D1 | D0 | — | — | — | — |
| ADRH | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 |

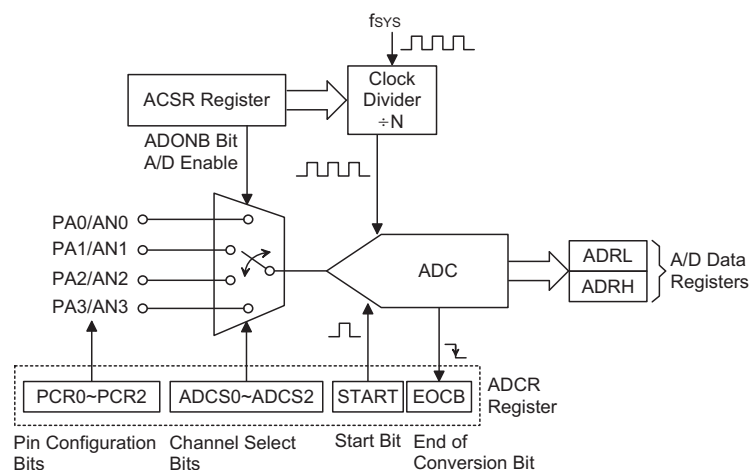
A/D Data Registers

A/D Converter Control Registers – ADCR, ACSR

To control the function and operation of the A/D converter, two control registers known as ADCR and ACSR are provided. These 8-bit registers define functions such as the selection of which analog channel is connected to the internal A/D converter, which pins are used as analog inputs and which are used as normal I/Os, the A/D clock source as well as controlling the start function and monitoring the A/D converter end of conversion status.

The ACS2~ACS0 bits in the ADCR register define the channel number. As the device contains only one actual analog to digital converter circuit, each of the individual 8 analog inputs must be routed to the converter. It is the function of the ACS2~ACS0 bits in the ADCR register to determine which analog channel is actually connected to the internal A/D converter.

The ADCR control register also contains the PCR2~PCR0 bits which determine which pins on PA0~PA3 are used as analog inputs for the A/D converter and which pins are to be used as normal I/O pins. If the 3-bit address on PCR2~PCR0 has a value of "111", then pins, namely AN0~AN3 will all be set as analog inputs. Note that if the PCR2~PCR0 bits are all set to zero, then all the PA0~PA3 pins will be setup as normal I/Os.



A/D Converter Structure

• ADRH, ADRL Register

| Bit | ADRH | | | | | | | | ADRL | | | | | | | |
|------|------|-----|----|----|----|----|----|----|------|----|----|----|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | — | — | — | — |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | — | — | — | — |
| POR | x | x | x | x | x | x | x | x | x | x | x | x | — | — | — | — |

"x" unknown

unimplemented, read as "0"

D11~D0: ADC conversion data

• ADCR Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------|------|------|------|------|------|------|------|
| Name | START | EOCB | PCR2 | PCR1 | PCR0 | ACS2 | ACS1 | ACS0 |
| R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

- Bit 7 **START**: Start the A/D conversion
 0→1→0 : start
 0→1 : reset the A/D converter and set EOCB to "1"
- Bit 6 **EOCB**: End of A/D conversion flag
 0: A/D conversion ended
 1: A/D conversion in progress
- Bit 5~3 **PCR2~PCR0**: A/D channel configuration
 000 A/D channel all off - ADC module power down
 001 PA0 enabled as AN0
 010 PA0~PA1 enabled as AN0~AN1
 011 PA0~PA2 enabled as AN0~AN2
 1xx PA0~PA3 enabled as AN0~AN3
- Bit 2~0 **ACS2~ACS0**: Select A/D channel
 000 AN0
 001 AN1
 010 AN2
 011 AN3
 1xx undefined, can't be used

• ACSR Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|-------|---|---|---|-------|-------|-------|
| Name | TEST | ADONB | — | — | — | ADCS2 | ADCS1 | ADCS0 |
| R/W | R/W | R/W | — | — | — | R/W | R/W | R/W |
| POR | 1 | 0 | — | — | — | 0 | 0 | 0 |

Bit 7 **TEST:** for test mode use only

Bit 6 **ADONB:** ADC module power on/off control bit
 0: ADC module power on
 1: ADC module power off
 Note: 1. it is recommended to set ADONB=1 before entering sleep for saving power.
 2. ADONB=1 will power down the ADC module.

Bit 5~3 unimplemented, read as "0"

Bit 2~0 **ADCS2~ADCS0:** Select A/D converter clock source
 000: system clock/2
 001: system clock/8
 010: system clock/32
 011: undefined, can't be used.
 100: system clock
 101: system clock/4
 110: system clock/16
 111: undefined, can't be used.

The START bit in the register is used to start and reset the A/D converter. When the microcontroller sets this bit from low to high and then low again, an analog to digital conversion cycle will be initiated. When the START bit is brought from low to high but not low again, the EOCB bit in the ADCR register will be set to a "1" and the analog to digital converter will be reset. It is the START bit that is used to control the overall start operation of the internal analog to digital converter.

The EOCB bit in the ADCR register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set to "0" by the microcontroller after a conversion cycle has ended. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can be used to poll the EOCB bit in the ADCR register to check whether it has been cleared as an alternative method of detecting the end of an A/D conversion cycle.

The clock source for the A/D converter, which originates from the system clock f_{SYS} , is first divided by a division ratio, the value of which is determined by the ADCS2, ADCS1 and ADCS0 bits in the ACSR register.

Controlling the power on/off function of the A/D converter circuitry is implemented using the value of the ADONB bit.

Although the A/D clock source is determined by the system clock f_{SYS} , and by bits ADCS2, ADCS1 and ADCS0, there are some limitations on the maximum A/D clock source speed that can be selected. As the minimum value of permissible A/D clock period, t_{AD} , is 0.5 μ s, care must be taken for system clock speeds in excess of 4MHz. For system clock speeds in excess of 4MHz, the ADCS2, ADCS1 and ADCS0 bits should not be set to "000". Doing so will give A/D clock periods that are less than the minimum A/D clock period which may result in inaccurate A/D conversion values. Refer to the following table for examples, where values marked with an asterisk * show where, depending upon the device, special care must be taken, as the values may be less than the specified minimum A/D Clock Period.

| f_{sys} | A/D Clock Period (t_{AD}) | | | | | | |
|-----------|-----------------------------------------|-----------------------------------------|------------------------------------------|---------------------------------------|-----------------------------------------|------------------------------------------|------------------------------|
| | ADCS2, ADCS1, ADCS0=000 ($f_{sys}/2$) | ADCS2, ADCS1, ADCS0=001 ($f_{sys}/8$) | ADCS2, ADCS1, ADCS0=010 ($f_{sys}/32$) | ADCS2, ADCS1, ADCS0=100 (f_{sys}) | ADCS2, ADCS1, ADCS0=101 ($f_{sys}/4$) | ADCS2, ADCS1, ADCS0=110 ($f_{sys}/16$) | ADCS2, ADCS1, ADCS0=011, 111 |
| 1MHz | 2 μ s | 8 μ s | 32 μ s | 1 μ s | 4 μ s | 16 μ s | Undefined |
| 2MHz | 1 μ s | 4 μ s | 16 μ s | 500ns | 2 μ s | 8 μ s | Undefined |
| 4MHz | 500ns | 2 μ s | 8 μ s | 250ns* | 1 μ s | 4 μ s | Undefined |
| 8MHz | 250ns* | 1 μ s | 4 μ s | 125ns* | 500ns | 2 μ s | Undefined |
| 12MHz | 167ns* | 667ns | 2.67 μ s | 83ns* | 333ns* | 1 μ s | Undefined |

A/D Clock Period Examples

A/D Input Pins

All of the A/D analog input pins are pin-shared with the I/O pins on Port A. Bits PCR2~PCR0 in the register, determine whether the input pins are setup as normal Port A input/output pins or whether they are setup as analog inputs. In this way, pins can be changed under program control to change their function from normal I/O operation to analog inputs and vice versa. Pull-high resistors, which are setup through register programming, apply to the input pins only when they are used as normal I/O pins, if setup as A/D inputs the pull-high resistors will be automatically disconnected. Note that it is not necessary to first setup the A/D pin as an input in the PBC port control register to enable the A/D input as when the PCR2~PCR0 bits enable an A/D input, the status of the port control register will be overridden.

Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1
Select the required A/D conversion clock by correctly programming bits ADCS2, ADCS1 and ADCS0 in the register.
- Step 2
Select which pins are to be used as A/D inputs and configure them as A/D input pins by correctly programming the PCR2~PCR0 bits in the ADCR register.
- Step 3
Enable the A/D by clearing the ADONB in the ACSR register to zero.
- Step 4
Select which channel is to be connected to the internal A/D converter by correctly programming the ACS2~ACS0 bits which are also contained in the register.

- Step 5
If the interrupts are to be used, the interrupt control registers must be correctly configured to ensure the A/D converter interrupt function is active. The master interrupt control bit, EMI, the INTC0 interrupt control register must be set to "1", the A/D converter interrupt bit, ADE, must also be set to "1".

- Step 6
The analog to digital conversion process can now be initialised by setting the START bit in the ADCR register from "0" to "1" and then to "0" again. Note that this bit should have been originally set to "0".

- Step 7
To check when the analog to digital conversion process is complete, the EOCB bit in the ADCR register can be polled. The conversion process is complete when this bit goes low. When this occurs the A/D data registers ADRL and ADRH can be read to obtain the conversion value. As an alternative method if the interrupts are enabled and the stack is not full, the program can wait for an A/D interrupt to occur.

Note: When checking for the end of the conversion process, if the method of polling the EOCB bit in the ADCR register is used, the interrupt enable step above can be omitted.

The accompanying diagram shows graphically the various stages involved in an analog to digital conversion process and its associated timing.

The setting up and operation of the A/D converter function is fully under the control of the application program as there are no configuration options associated with the A/D converter. After an A/D conversion process has been initiated by the application program, the microcontroller internal hardware will begin to carry out the conversion, during which time the program can continue with other functions. The time taken for the A/D conversion is $16t_{AD}$ where t_{AD} is equal to the A/D clock period.

Programming Considerations

When programming, special attention must be given to the PCR[2:0] bits in the register. If these bits are all cleared to zero no external pins will be selected for use as A/D input pins allowing the pins to be used as normal I/O pins. When this happens the internal A/D circuitry will be power down. Setting the ADONB bit high has the ability to power down the internal A/D circuitry, which may be an important consideration in power sensitive applications.

A/D Transfer Function

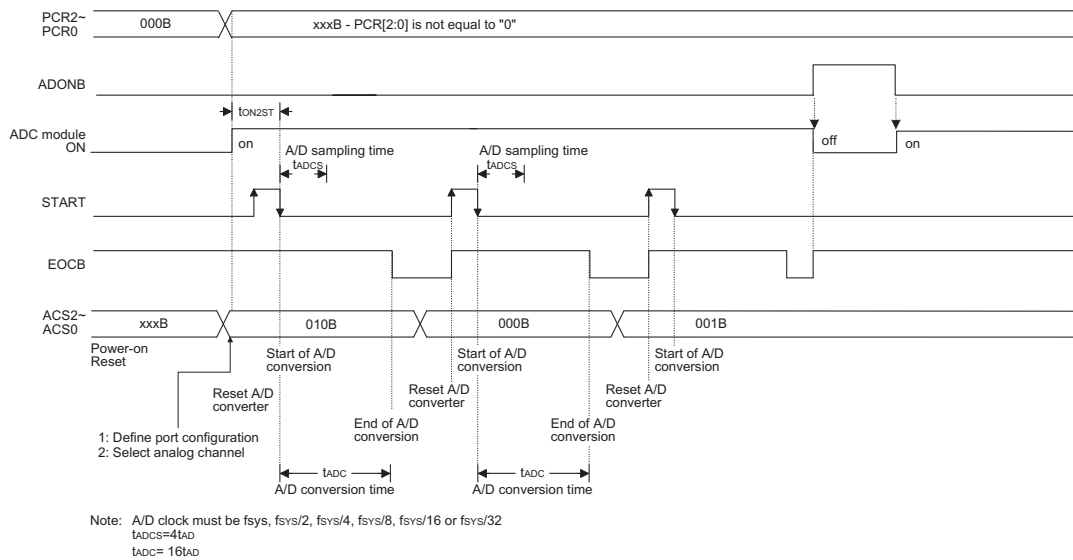
As the device contain a 12-bit A/D converter, its full-scale converted digitised value is equal to FFFH. Since the full-scale analog input value is equal to the V_{DD} voltage, this gives a single bit analog input value of V_{DD}/4096. The diagram show the ideal transfer function

between the analog input value and the digitised output value for the A/D converter.

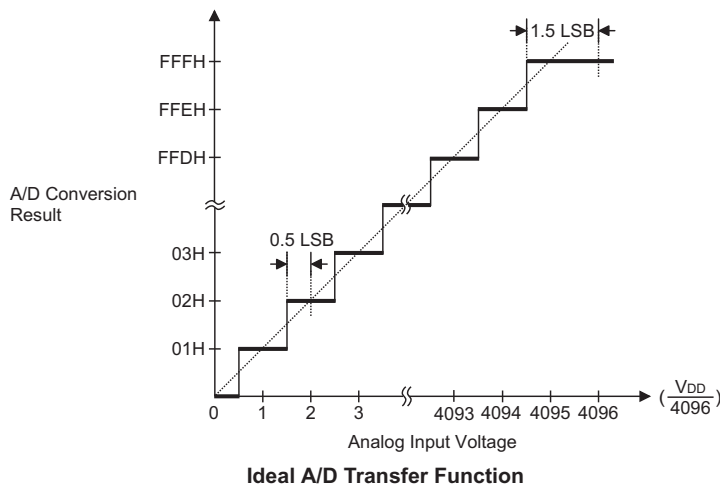
Note that to reduce the quantisation error, a 0.5 LSB offset is added to the A/D Converter input. Except for the digitised zero value, the subsequent digitised values will change at a point 0.5 LSB below where they would change without the offset, and the last full scale digitised value will change at a point 1.5 LSB below the V_{DD} level.

A/D Programming Example

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the EOCB bit in the ADCR register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.



A/D Conversion Timing



Example: using an EOCB polling method to detect the end of conversion

```

clr EADI ; disable ADC interrupt
mov a,00000001B
mov ACSR,a ; select fsys/8 as A/D clock and ADONB=0
mov a,00100000B ; setup ADCR register to configure Port as A/D inputs
mov ADCR,a ; and select AN0 to be connected to the A/D converter
:
:
Start_conversion:
clr START
set START ; reset A/D
clr START ; start A/D
Polling_EOCB:
sz EOCB ; poll the ADCR register EOCB bit to detect end
; of A/D conversion
jmp polling_EOCB ; continue polling
mov a,ADRL ; read low byte conversion result value
mov adrl_buffer,a ; save result to user defined register
mov a,ADRH ; read high byte conversion result value
mov adrh_buffer,a ; save result to user defined register
:
jmp start_conversion ; start next A/D conversion

```

Note: To power off ADC module, it is necessary to set ADONB as "1".

Example: using the interrupt method to detect the end of conversion

```

clr EADI ; disable ADC interrupt
mov a,00000001B
mov ACSR,a ; select fsys/8 as A/D clock and ADONB=0
mov a,00100000B ; setup ADCR register to configure Port as A/D inputs
mov ADCR,a ; and select AN0 to be connected to the A/D
:
:
Start_conversion:
clr START
set START ; reset A/D
clr START ; start A/D
clr ADF ; clear ADC interrupt request flag
set EADI ; enable ADC interrupt
set EMI ; enable global interrupt
:
:
:
; ADC interrupt service routine
ADC_:
mov acc_stack,a ; save ACC to user defined memory
mov a,STATUS
mov status_stack,a ; save STATUS to user defined memory
:
:
mov a,ADRL ; read low byte conversion result value
mov adrl_buffer,a ; save result to user defined register
mov a,ADRH ; read high byte conversion result value
mov adrh_buffer,a ; save result to user defined register
:
:
EXIT_ISR:
mov a,status_stack
mov STATUS,a ; restore STATUS from user defined memory
mov a,acc_stack ; restore ACC from user defined memory
clr ADF ; clear ADC interrupt flag
reti

```

Note: To power off ADC module, it is necessary to set ADONB as "1".

Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer/Event Counter or Time Base requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs.

The devices contain a single external interrupt and multiple internal interrupts. The external interrupt is controlled by the action of the external interrupt pin, while the internal interrupt is controlled by the Timer/Event Counters and Time Base overflows.

Interrupt Register

Overall interrupt control, which means interrupt enabling and request flag setting, is controlled by using two registers, INTC0 and INTC1. By controlling the appropriate enable bits in this registers each individual interrupt can be enabled or disabled. Also when an interrupt occurs, the corresponding request flag will be set by the microcontroller. The global enable flag if cleared to zero will disable all interrupts.

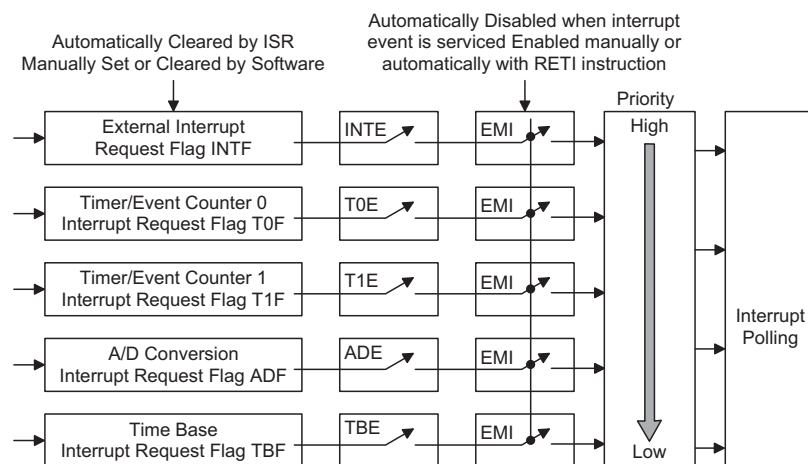
Interrupt Operation

A Timer/Event Counter overflow, a Time Base event or an active edge on the external interrupt pin will all generate an interrupt request by setting their corresponding request flag, if their appropriate interrupt enable bit is set. When this happens, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program

Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a JMP statement which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a RETI instruction, which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

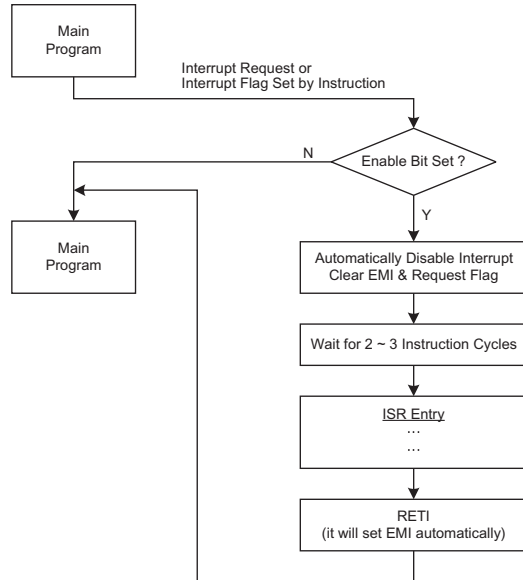
The various interrupt enable bits, together with their associated request flags, are shown in the following diagram with their order of priority.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded. If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full.



Interrupt Scheme

When an interrupt request is generated it takes 2 or 3 instruction cycle before the program jumps to the interrupt vector. If the device is in the Sleep Mode and is woken up by an interrupt request then it will take 3 cycles before the program jumps to the interrupt vector.



Interrupt Flow

Interrupt Priority

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In case of simultaneous requests, the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

| Interrupt Source | Priority | Vector |
|--------------------------------|----------|--------|
| External Interrupt | 1 | 04H |
| Timer/Event Counter 0 Overflow | 2 | 08H |
| Timer/Event Counter 1 Overflow | 3 | 0CH |
| A/D Conversion Complete | 4 | 10H |
| Time Base Overflow | 5 | 14H |

In cases where both external and internal interrupts are enabled and where an external and internal interrupt occurs simultaneously, the external interrupt will always have priority and will therefore be serviced first. Suitable masking of the individual interrupts using the interrupt registers can prevent simultaneous occurrences.

External Interrupt

For an external interrupt to occur, the global interrupt enable bit, EMI, and external interrupt enable bit, INTE, must first be set. An actual external interrupt will take place when the external interrupt request flag, INTF, is set, a situation that will occur when an edge transition appears on the external INT line. The type of transition that will trigger an external interrupt, whether high to low, low to high or both is determined by the INTEG0 and INTEG1 bits, which are bits 6 and 7 respectively, in the CTRL1 control register. These two bits can also disable the external interrupt function.

| INTEG1 | INTEG0 | Edge Trigger Type |
|--------|--------|----------------------------|
| 0 | 0 | External interrupt disable |
| 0 | 1 | Rising edge Trigger |
| 1 | 0 | Falling edge Trigger |
| 1 | 1 | Both edge Trigger |

The external interrupt pin is pin-shared with the I/O pin PA3 and can only be configured as an external interrupt pin if the corresponding external interrupt enable bit in the INTC0 register has been set and the edge trigger type has been selected using the CTRL1 register. The pin must also be setup as an input by setting the corresponding PAC.3 bit in the port control register. When the interrupt is enabled, the stack is not full and a transition appears on the external interrupt pin, a subroutine call to the external interrupt vector at location 04H, will take place. When the interrupt is serviced, the external interrupt request flag, INTF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor connections on this pin will remain valid even if the pin is used as an external interrupt input.

• INTC0 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|-----|-----|------|-----|-----|------|-----|
| Name | — | T1F | T0F | INTF | T1E | T0E | INTE | EMI |
| R/W | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- Bit 7 unimplemented, read as "0"
- Bit 6 **T1F**: Timer/Event Counter 1 interrupt request flag
0: inactive
1: active
- Bit 5 **T0F**: Timer/Event Counter 0 interrupt request flag
0: inactive
1: active
- Bit 4 **INTF**: External interrupt request flag
0: inactive
1: active
- Bit 3 **T1E**: Timer/Event Counter 1 interrupt enable
0: disable
1: enable
- Bit 2 **T0E**: Timer/Event Counter 0 interrupt enable
0: disable
1: enable
- Bit 1 **INTE**: external interrupt enable
0: disable
1: enable
- Bit 0 **EMI**: Master interrupt global enable
0: disable
1: enable

• INTC1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|-----|-----|---|---|-----|-----|
| Name | — | — | TBF | ADF | — | — | TBE | ADE |
| R/W | — | — | R/W | R/W | — | — | R/W | R/W |
| POR | — | — | 0 | 0 | — | — | 0 | 0 |

- Bit 7~6,3~2 unimplemented, read as "0"
- Bit 5 **TBF**: Time Base event interrupt request flag
0: inactive
1: active
- Bit 4 **ADF**: A/D Conversion interrupt request flag
0: inactive
1: active
- Bit 1 **TBE**: Time base event interrupt enable
0: disable
1: enable
- Bit 0 **ADE**: A/D Conversion interrupt enable
0: disable
1: enable

Timer/Event Counter Interrupt

For a Timer/Event Counter interrupt to occur, the global interrupt enable bit, EMI, and the corresponding timer interrupt enable bit, TnE, must first be set. An actual Timer/Event Counter interrupt will take place when the Timer/Event Counter request flag, TnF, is set, a situation that will occur when the relevant Timer/Event Counter overflows. When the interrupt is enabled, the stack is not full and a Timer/Event Counter n overflow occurs, a subroutine call to the relevant timer interrupt vector, will take place. When the interrupt is serviced, the timer interrupt request flag, TnF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Time Base Interrupt

For a time base interrupt to occur the global interrupt enable bit EMI and the corresponding interrupt enable bit TBE, must first be set. An actual Time Base interrupt will take place when the time base request flag TBF is set, a situation that will occur when the Time Base overflows. When the interrupt is enabled, the stack is not full and a time base overflow occurs a subroutine call to time base vector will take place. When the interrupt is serviced, the time base interrupt flag, TBF will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Programming Considerations

By disabling the interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by a software instruction.

It is recommended that programs do not use the "CALL subroutine" instruction within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a "CALL subroutine" is executed in the interrupt subroutine.

All of these interrupts have the capability of waking up the processor when in the Sleep Mode.

Only the Program Counter is pushed onto the stack. If the contents of the register or status register are altered by the interrupt service program, which may corrupt the desired control sequence, then the contents should be saved in advance.

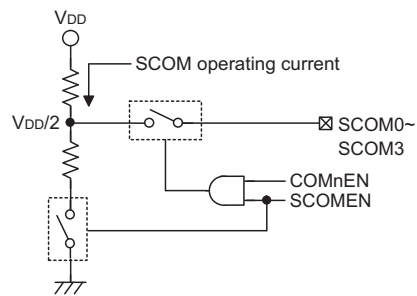
SCOM Function for LCD

The devices have the capability of driving external LCD panels. The common pins for LCD driving, SCOM0~SCOM3, are pin shared with certain pin on the PB0~PB3 port. The LCD signals (COM and SEG) are generated using the application program.

LCD Operation

An external LCD panel can be driven using this device by configuring the PB0~PB3 pins as common pins and using other output ports lines as segment pins. The LCD driver function is controlled using the SCOMC register which in addition to controlling the overall on/off function also controls the bias voltage setup function. This enables the LCD COM driver to generate the necessary $V_{DD}/2$ voltage levels for LCD 1/2 bias operation.

The SCOMEN bit in the SCOMC register is the overall master control for the LCD Driver, however this bit is used in conjunction with the COMnEN bits to select which Port B pins are used for LCD driving. Note that the Port Control register does not need to first setup the pins as outputs to enable the LCD driver operation.



LCD COM Bias

| SCOMEN | COMnEN | Pin Function | O/P Level |
|--------|--------|--------------|------------|
| 0 | X | I/O | 0 or 1 |
| 1 | 0 | I/O | 0 or 1 |
| 1 | 1 | SCOMN | $V_{DD}/2$ |

Output Control

LCD Bias Control

The LCD COM driver enables a range of selections to be provided to suit the requirement of the LCD panel which is being used. The bias resistor choice is implemented using the ISEL1 and ISEL0 bits in the SCOMC register.

• SCOMC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-------|-------|--------|--------|--------|--------|--------|
| Name | — | ISEL1 | ISEL0 | SCOMEN | COM3EN | COM2EN | COM1EN | COM0EN |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

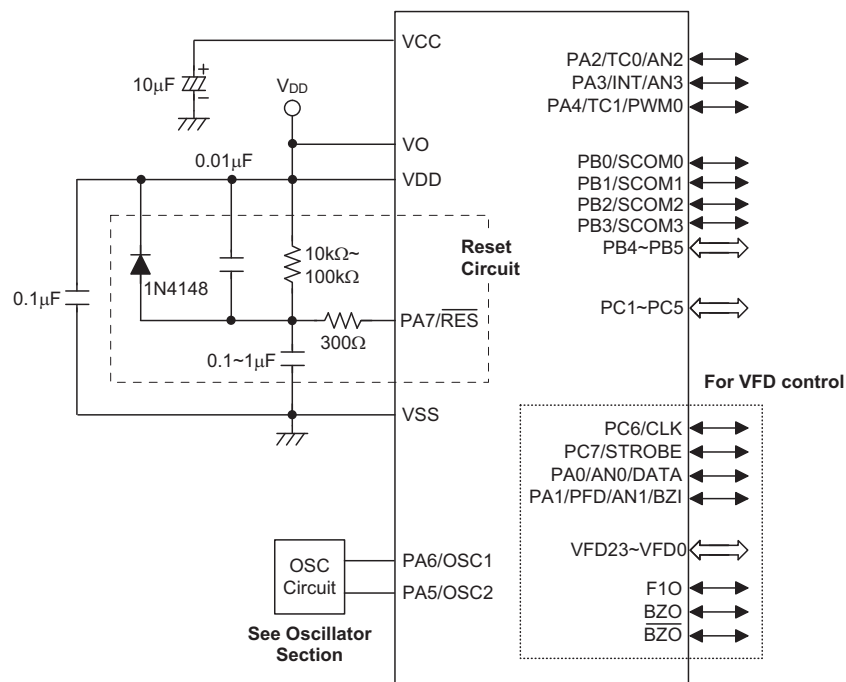
- Bit 7 **Reserved Bit**
 1: Unpredictable operation - bit must NOT be set high
 0: Correct level - bit must be reset to zero for correct operation
- Bit 6,5 **ISEL1, ISEL0**: SCOM operating current selection ($V_{DD}=5V$)
 00: 25 μ A
 01: 50 μ A
 10: 100 μ A
 11: 200 μ A
- Bit 4 **SCOMEN**: SCOM module on/off control
 0: disable
 1: enable
 SCOMn can be enable by COMnEN if SCOMEN=1
- Bit 3 **COM3EN**: PB3 or SCOM3 selection
 0: GPIO
 1: SCOM3
- Bit 2 **COM2EN**: PB2 or SCOM2 selection
 0: GPIO
 1: SCOM2
- Bit 1 **COM1EN**: PB1 or SCOM1 selection
 0: GPIO
 1: SCOM1
- Bit 0 **COM0EN**: PB0 or SCOM0 selection
 0: GPIO
 1: SCOM0

Configuration Options

Configuration options refer to certain options within the MCU that are programmed into the OTP Program Memory device during the programming process. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the device using the hardware programming tools, once they are selected they cannot be changed later by the application software. All options must be defined for proper system function, the details of which are shown in the table.

| No. | Options |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | Watchdog Timer: enable or disable |
| 2 | Watchdog Timer clock source: LXT, LIRC or $f_{SYS}/4$ Note: LXT oscillator must be selected by OSC configuration option if WDT clock source is from LXT. |
| 3 | CLRWDT instructions: 1 or 2 instructions |
| 4 | System oscillator configuration: HXT, HIRC, ERC, HIRC + LXT |
| 5 | LVR function: enable or disable |
| 6 | LVR voltage: 2.1V, 3.15V or 4.2V |
| 7 | \overline{RES} or PA7 pin function |
| 8 | SST: 1024 or 2 clocks (determine t_{SST} for HIRC/ERC) |
| 9 | Internal RC: 4MHz, 8MHz or 12MHz |

Application Circuits



Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontrollers, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5 μ s and branch or call instructions would be implemented within 1 μ s. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and

subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operations

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application where rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction RET in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table conventions:

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0-7 number of bits

addr: Program memory address

| Mnemonic | Description | Cycles | Flag Affected |
|----------------------------------|-----------------------------------------------------------------|-------------------|---------------|
| Arithmetic | | | |
| ADD A,[m] | Add Data Memory to ACC | 1 | Z, C, AC, OV |
| ADDM A,[m] | Add ACC to Data Memory | ¹ Note | Z, C, AC, OV |
| ADD A,x | Add immediate data to ACC | 1 | Z, C, AC, OV |
| ADC A,[m] | Add Data Memory to ACC with Carry | 1 | Z, C, AC, OV |
| ADCM A,[m] | Add ACC to Data memory with Carry | ¹ Note | Z, C, AC, OV |
| SUB A,x | Subtract immediate data from the ACC | 1 | Z, C, AC, OV |
| SUB A,[m] | Subtract Data Memory from ACC | 1 | Z, C, AC, OV |
| SUBM A,[m] | Subtract Data Memory from ACC with result in Data Memory | ¹ Note | Z, C, AC, OV |
| SBC A,[m] | Subtract Data Memory from ACC with Carry | 1 | Z, C, AC, OV |
| SBCM A,[m] | Subtract Data Memory from ACC with Carry, result in Data Memory | ¹ Note | Z, C, AC, OV |
| DAA [m] | Decimal adjust ACC for Addition with result in Data Memory | ¹ Note | C |
| Logic Operation | | | |
| AND A,[m] | Logical AND Data Memory to ACC | 1 | Z |
| OR A,[m] | Logical OR Data Memory to ACC | 1 | Z |
| XOR A,[m] | Logical XOR Data Memory to ACC | 1 | Z |
| ANDM A,[m] | Logical AND ACC to Data Memory | ¹ Note | Z |
| ORM A,[m] | Logical OR ACC to Data Memory | ¹ Note | Z |
| XORM A,[m] | Logical XOR ACC to Data Memory | ¹ Note | Z |
| AND A,x | Logical AND immediate Data to ACC | 1 | Z |
| OR A,x | Logical OR immediate Data to ACC | 1 | Z |
| XOR A,x | Logical XOR immediate Data to ACC | 1 | Z |
| CPL [m] | Complement Data Memory | ¹ Note | Z |
| CPLA [m] | Complement Data Memory with result in ACC | 1 | Z |
| Increment & Decrement | | | |
| INCA [m] | Increment Data Memory with result in ACC | 1 | Z |
| INC [m] | Increment Data Memory | ¹ Note | Z |
| DECA [m] | Decrement Data Memory with result in ACC | 1 | Z |
| DEC [m] | Decrement Data Memory | ¹ Note | Z |

| Mnemonic | Description | Cycles | Flag Affected |
|----------------------|-----------------------------------------------------------|-------------------|---------------|
| Rotate | | | |
| RRA [m] | Rotate Data Memory right with result in ACC | 1 | None |
| RR [m] | Rotate Data Memory right | ¹ Note | None |
| RRCA [m] | Rotate Data Memory right through Carry with result in ACC | 1 | C |
| RRC [m] | Rotate Data Memory right through Carry | ¹ Note | C |
| RLA [m] | Rotate Data Memory left with result in ACC | 1 | None |
| RL [m] | Rotate Data Memory left | ¹ Note | None |
| RLCA [m] | Rotate Data Memory left through Carry with result in ACC | 1 | C |
| RLC [m] | Rotate Data Memory left through Carry | ¹ Note | C |
| Data Move | | | |
| MOV A,[m] | Move Data Memory to ACC | 1 | None |
| MOV [m],A | Move ACC to Data Memory | ¹ Note | None |
| MOV A,x | Move immediate data to ACC | 1 | None |
| Bit Operation | | | |
| CLR [m].i | Clear bit of Data Memory | ¹ Note | None |
| SET [m].i | Set bit of Data Memory | ¹ Note | None |
| Branch | | | |
| JMP addr | Jump unconditionally | 2 | None |
| SZ [m] | Skip if Data Memory is zero | ¹ Note | None |
| SZA [m] | Skip if Data Memory is zero with data movement to ACC | ¹ note | None |
| SZ [m].i | Skip if bit i of Data Memory is zero | ¹ Note | None |
| SNZ [m].i | Skip if bit i of Data Memory is not zero | ¹ Note | None |
| SIZ [m] | Skip if increment Data Memory is zero | ¹ Note | None |
| SDZ [m] | Skip if decrement Data Memory is zero | ¹ Note | None |
| SIZA [m] | Skip if increment Data Memory is zero with result in ACC | ¹ Note | None |
| SDZA [m] | Skip if decrement Data Memory is zero with result in ACC | ¹ Note | None |
| CALL addr | Subroutine call | 2 | None |
| RET | Return from subroutine | 2 | None |
| RET A,x | Return from subroutine and load immediate data to ACC | 2 | None |
| RETI | Return from interrupt | 2 | None |
| Table Read | | | |
| TABRDC [m] | Read table (current page) to TBLH and Data Memory | ² Note | None |
| TABRDL [m] | Read table (last page) to TBLH and Data Memory | ² Note | None |
| Miscellaneous | | | |
| NOP | No operation | 1 | None |
| CLR [m] | Clear Data Memory | ¹ Note | None |
| SET [m] | Set Data Memory | ¹ Note | None |
| CLR WDT | Clear Watchdog Timer | 1 | TO, PDF |
| CLR WDT1 | Pre-clear Watchdog Timer | 1 | TO, PDF |
| CLR WDT2 | Pre-clear Watchdog Timer | 1 | TO, PDF |
| SWAP [m] | Swap nibbles of Data Memory | ¹ Note | None |
| SWAPA [m] | Swap nibbles of Data Memory with result in ACC | 1 | None |
| HALT | Enter power down mode | 1 | TO, PDF |

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.
2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.
3. For the "CLR WDT1" and "CLR WDT2" instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both "CLR WDT1" and "CLR WDT2" instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

| | |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| ADC A,[m] | Add Data Memory to ACC with Carry |
| Description | The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC + [m] + C$ |
| Affected flag(s) | OV, Z, AC, C |
| ADCM A,[m] | Add ACC to Data Memory with Carry |
| Description | The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory. |
| Operation | $[m] \leftarrow ACC + [m] + C$ |
| Affected flag(s) | OV, Z, AC, C |
| ADD A,[m] | Add Data Memory to ACC |
| Description | The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC + [m]$ |
| Affected flag(s) | OV, Z, AC, C |
| ADD A,x | Add immediate data to ACC |
| Description | The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC + x$ |
| Affected flag(s) | OV, Z, AC, C |
| ADDM A,[m] | Add ACC to Data Memory |
| Description | The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory. |
| Operation | $[m] \leftarrow ACC + [m]$ |
| Affected flag(s) | OV, Z, AC, C |
| AND A,[m] | Logical AND Data Memory to ACC |
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC \text{ "AND" } [m]$ |
| Affected flag(s) | Z |
| AND A,x | Logical AND immediate data to ACC |
| Description | Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC \text{ "AND" } x$ |
| Affected flag(s) | Z |
| ANDM A,[m] | Logical AND ACC to Data Memory |
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory. |
| Operation | $[m] \leftarrow ACC \text{ "AND" } [m]$ |
| Affected flag(s) | Z |

| | |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CALL addr | Subroutine call |
| Description | Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction. |
| Operation | Stack ← Program Counter + 1 Program Counter ← addr |
| Affected flag(s) | None |
| CLR [m] | Clear Data Memory |
| Description | Each bit of the specified Data Memory is cleared to 0. |
| Operation | [m] ← 00H |
| Affected flag(s) | None |
| CLR [m].i | Clear bit of Data Memory |
| Description | Bit i of the specified Data Memory is cleared to 0. |
| Operation | [m].i ← 0 |
| Affected flag(s) | None |
| CLR WDT | Clear Watchdog Timer |
| Description | The TO, PDF flags and the WDT are all cleared. |
| Operation | WDT cleared TO ← 0 PDF ← 0 |
| Affected flag(s) | TO, PDF |
| CLR WDT1 | Pre-clear Watchdog Timer |
| Description | The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repeatedly executing this instruction without alternately executing CLR WDT2 will have no effect. |
| Operation | WDT cleared TO ← 0 PDF ← 0 |
| Affected flag(s) | TO, PDF |
| CLR WDT2 | Pre-clear Watchdog Timer |
| Description | The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repeatedly executing this instruction without alternately executing CLR WDT1 will have no effect. |
| Operation | WDT cleared TO ← 0 PDF ← 0 |
| Affected flag(s) | TO, PDF |

| | |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPL [m] | Complement Data Memory |
| Description | Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. |
| Operation | $[m] \leftarrow \overline{[m]}$ |
| Affected flag(s) | Z |
| CPLA [m] | Complement Data Memory with result in ACC |
| Description | Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow \overline{[m]}$ |
| Affected flag(s) | Z |
| DAA [m] | Decimal-Adjust ACC for addition with result in Data Memory |
| Description | Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition. |
| Operation | $[m] \leftarrow ACC + 00H$ or $[m] \leftarrow ACC + 06H$ or $[m] \leftarrow ACC + 60H$ or $[m] \leftarrow ACC + 66H$ |
| Affected flag(s) | C |
| DEC [m] | Decrement Data Memory |
| Description | Data in the specified Data Memory is decremented by 1. |
| Operation | $[m] \leftarrow [m] - 1$ |
| Affected flag(s) | Z |
| DECA [m] | Decrement Data Memory with result in ACC |
| Description | Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow [m] - 1$ |
| Affected flag(s) | Z |
| HALT | Enter power down mode |
| Description | This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared. |
| Operation | $TO \leftarrow 0$ $PDF \leftarrow 1$ |
| Affected flag(s) | TO, PDF |

| | |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INC [m] | Increment Data Memory |
| Description | Data in the specified Data Memory is incremented by 1. |
| Operation | $[m] \leftarrow [m] + 1$ |
| Affected flag(s) | Z |
| INCA [m] | Increment Data Memory with result in ACC |
| Description | Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC \leftarrow [m] + 1$ |
| Affected flag(s) | Z |
| JMP addr | Jump unconditionally |
| Description | The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction. |
| Operation | $Program\ Counter \leftarrow addr$ |
| Affected flag(s) | None |
| MOV A,[m] | Move Data Memory to ACC |
| Description | The contents of the specified Data Memory are copied to the Accumulator. |
| Operation | $ACC \leftarrow [m]$ |
| Affected flag(s) | None |
| MOV A,x | Move immediate data to ACC |
| Description | The immediate data specified is loaded into the Accumulator. |
| Operation | $ACC \leftarrow x$ |
| Affected flag(s) | None |
| MOV [m],A | Move ACC to Data Memory |
| Description | The contents of the Accumulator are copied to the specified Data Memory. |
| Operation | $[m] \leftarrow ACC$ |
| Affected flag(s) | None |
| NOP | No operation |
| Description | No operation is performed. Execution continues with the next instruction. |
| Operation | No operation |
| Affected flag(s) | None |
| OR A,[m] | Logical OR Data Memory to ACC |
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator. |
| Operation | $ACC \leftarrow ACC \text{ "OR" } [m]$ |
| Affected flag(s) | Z |

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| OR A,x | Logical OR immediate data to ACC |
| Description | Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC "OR" x |
| Affected flag(s) | Z |
| ORM A,[m] | Logical OR ACC to Data Memory |
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory. |
| Operation | [m] ← ACC "OR" [m] |
| Affected flag(s) | Z |
| RET | Return from subroutine |
| Description | The Program Counter is restored from the stack. Program execution continues at the restored address. |
| Operation | Program Counter ← Stack |
| Affected flag(s) | None |
| RET A,x | Return from subroutine and load immediate data to ACC |
| Description | The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address. |
| Operation | Program Counter ← Stack ACC ← x |
| Affected flag(s) | None |
| RETI | Return from interrupt |
| Description | The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program. |
| Operation | Program Counter ← Stack EMI ← 1 |
| Affected flag(s) | None |
| RL [m] | Rotate Data Memory left |
| Description | The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. |
| Operation | [m].(i+1) ← [m].i; (i = 0~6) [m].0 ← [m].7 |
| Affected flag(s) | None |
| RLA [m] | Rotate Data Memory left with result in ACC |
| Description | The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | ACC.(i+1) ← [m].i; (i = 0~6) ACC.0 ← [m].7 |
| Affected flag(s) | None |

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| RLC [m] | Rotate Data Memory left through Carry |
| Description | The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0. |
| Operation | $[m].(i+1) \leftarrow [m].i; (i = 0\sim6)$ $[m].0 \leftarrow C$ $C \leftarrow [m].7$ |
| Affected flag(s) | C |
| RLCA [m] | Rotate Data Memory left through Carry with result in ACC |
| Description | Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC.(i+1) \leftarrow [m].i; (i = 0\sim6)$ $ACC.0 \leftarrow C$ $C \leftarrow [m].7$ |
| Affected flag(s) | C |
| RR [m] | Rotate Data Memory right |
| Description | The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7. |
| Operation | $[m].i \leftarrow [m].(i+1); (i = 0\sim6)$ $[m].7 \leftarrow [m].0$ |
| Affected flag(s) | None |
| RRA [m] | Rotate Data Memory right with result in ACC |
| Description | Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC.i \leftarrow [m].(i+1); (i = 0\sim6)$ $ACC.7 \leftarrow [m].0$ |
| Affected flag(s) | None |
| RRC [m] | Rotate Data Memory right through Carry |
| Description | The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. |
| Operation | $[m].i \leftarrow [m].(i+1); (i = 0\sim6)$ $[m].7 \leftarrow C$ $C \leftarrow [m].0$ |
| Affected flag(s) | C |
| RRCA [m] | Rotate Data Memory right through Carry with result in ACC |
| Description | Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged. |
| Operation | $ACC.i \leftarrow [m].(i+1); (i = 0\sim6)$ $ACC.7 \leftarrow C$ $C \leftarrow [m].0$ |
| Affected flag(s) | C |

| | |
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| SBC A,[m] | Subtract Data Memory from ACC with Carry |
| Description | The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $ACC \leftarrow ACC - [m] - \bar{C}$ |
| Affected flag(s) | OV, Z, AC, C |
| SBCM A,[m] | Subtract Data Memory from ACC with Carry and result in Data Memory |
| Description | The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $[m] \leftarrow ACC - [m] - \bar{C}$ |
| Affected flag(s) | OV, Z, AC, C |
| SDZ [m] | Skip if decrement Data Memory is 0 |
| Description | The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $[m] \leftarrow [m] - 1$ Skip if $[m] = 0$ |
| Affected flag(s) | None |
| SDZA [m] | Skip if decrement Data Memory is zero with result in ACC |
| Description | The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction. |
| Operation | $ACC \leftarrow [m] - 1$ Skip if $ACC = 0$ |
| Affected flag(s) | None |
| SET [m] | Set Data Memory |
| Description | Each bit of the specified Data Memory is set to 1. |
| Operation | $[m] \leftarrow FFH$ |
| Affected flag(s) | None |
| SET [m].i | Set bit of Data Memory |
| Description | Bit i of the specified Data Memory is set to 1. |
| Operation | $[m].i \leftarrow 1$ |
| Affected flag(s) | None |

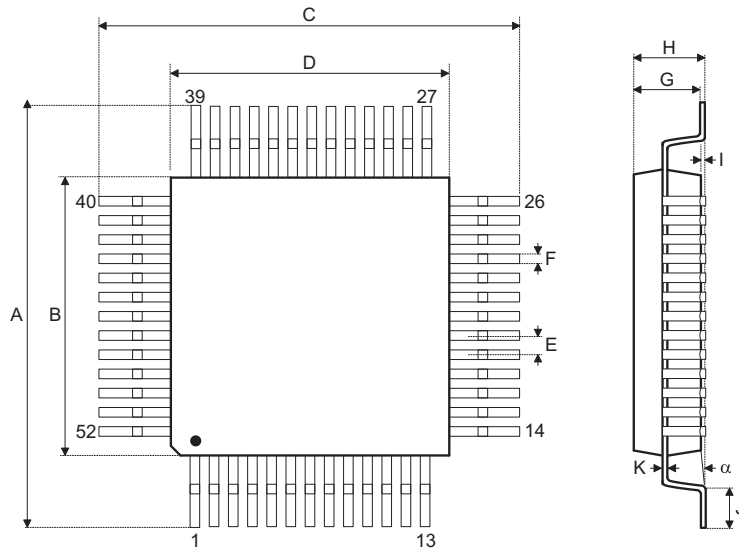
| | |
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| SIZ [m] | Skip if increment Data Memory is 0 |
| Description | The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $[m] \leftarrow [m] + 1$ Skip if $[m] = 0$ |
| Affected flag(s) | None |
| SIZA [m] | Skip if increment Data Memory is zero with result in ACC |
| Description | The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $ACC \leftarrow [m] + 1$ Skip if $ACC = 0$ |
| Affected flag(s) | None |
| SNZ [m].i | Skip if bit i of Data Memory is not 0 |
| Description | If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction. |
| Operation | Skip if $[m].i \neq 0$ |
| Affected flag(s) | None |
| SUB A,[m] | Subtract Data Memory from ACC |
| Description | The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $ACC \leftarrow ACC - [m]$ |
| Affected flag(s) | OV, Z, AC, C |
| SUBM A,[m] | Subtract Data Memory from ACC with result in Data Memory |
| Description | The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $[m] \leftarrow ACC - [m]$ |
| Affected flag(s) | OV, Z, AC, C |
| SUB A,x | Subtract immediate data from ACC |
| Description | The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1. |
| Operation | $ACC \leftarrow ACC - x$ |
| Affected flag(s) | OV, Z, AC, C |

| | |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SWAP [m] | Swap nibbles of Data Memory |
| Description | The low-order and high-order nibbles of the specified Data Memory are interchanged. |
| Operation | $[m].3 \sim [m].0 \leftrightarrow [m].7 \sim [m].4$ |
| Affected flag(s) | None |
| SWAPA [m] | Swap nibbles of Data Memory with result in ACC |
| Description | The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged. |
| Operation | $ACC.3 \sim ACC.0 \leftarrow [m].7 \sim [m].4$ $ACC.7 \sim ACC.4 \leftarrow [m].3 \sim [m].0$ |
| Affected flag(s) | None |
| SZ [m] | Skip if Data Memory is 0 |
| Description | If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | Skip if $[m] = 0$ |
| Affected flag(s) | None |
| SZA [m] | Skip if Data Memory is 0 with data movement to ACC |
| Description | The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction. |
| Operation | $ACC \leftarrow [m]$ Skip if $[m] = 0$ |
| Affected flag(s) | None |
| SZ [m].i | Skip if bit i of Data Memory is 0 |
| Description | If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction. |
| Operation | Skip if $[m].i = 0$ |
| Affected flag(s) | None |
| TABRDC [m] | Read table (current page) to TBLH and Data Memory |
| Description | The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH. |
| Operation | $[m] \leftarrow$ program code (low byte) $TBLH \leftarrow$ program code (high byte) |
| Affected flag(s) | None |
| TABRDL [m] | Read table (last page) to TBLH and Data Memory |
| Description | The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH. |
| Operation | $[m] \leftarrow$ program code (low byte) $TBLH \leftarrow$ program code (high byte) |
| Affected flag(s) | None |

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| XOR A,[m] | Logical XOR Data Memory to ACC |
| Description | Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC "XOR" [m] |
| Affected flag(s) | Z |
| XORM A,[m] | Logical XOR ACC to Data Memory |
| Description | Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory. |
| Operation | [m] ← ACC "XOR" [m] |
| Affected flag(s) | Z |
| XOR A,x | Logical XOR immediate data to ACC |
| Description | Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator. |
| Operation | ACC ← ACC "XOR" x |
| Affected flag(s) | Z |

Package Information

52-pin QFP (14mm×14mm) Outline Dimensions



| Symbol | Dimensions in mm | | |
|----------|------------------|------|-------|
| | Min. | Nom. | Max. |
| A | 17.30 | — | 17.50 |
| B | 13.90 | — | 14.10 |
| C | 17.30 | — | 17.50 |
| D | 13.90 | — | 14.10 |
| E | — | 1.00 | — |
| F | — | 0.40 | — |
| G | 2.50 | — | 3.10 |
| H | — | — | 3.40 |
| I | — | 0.10 | — |
| J | 0.73 | — | 1.03 |
| K | 0.10 | — | 0.20 |
| α | 0° | — | 7° |

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